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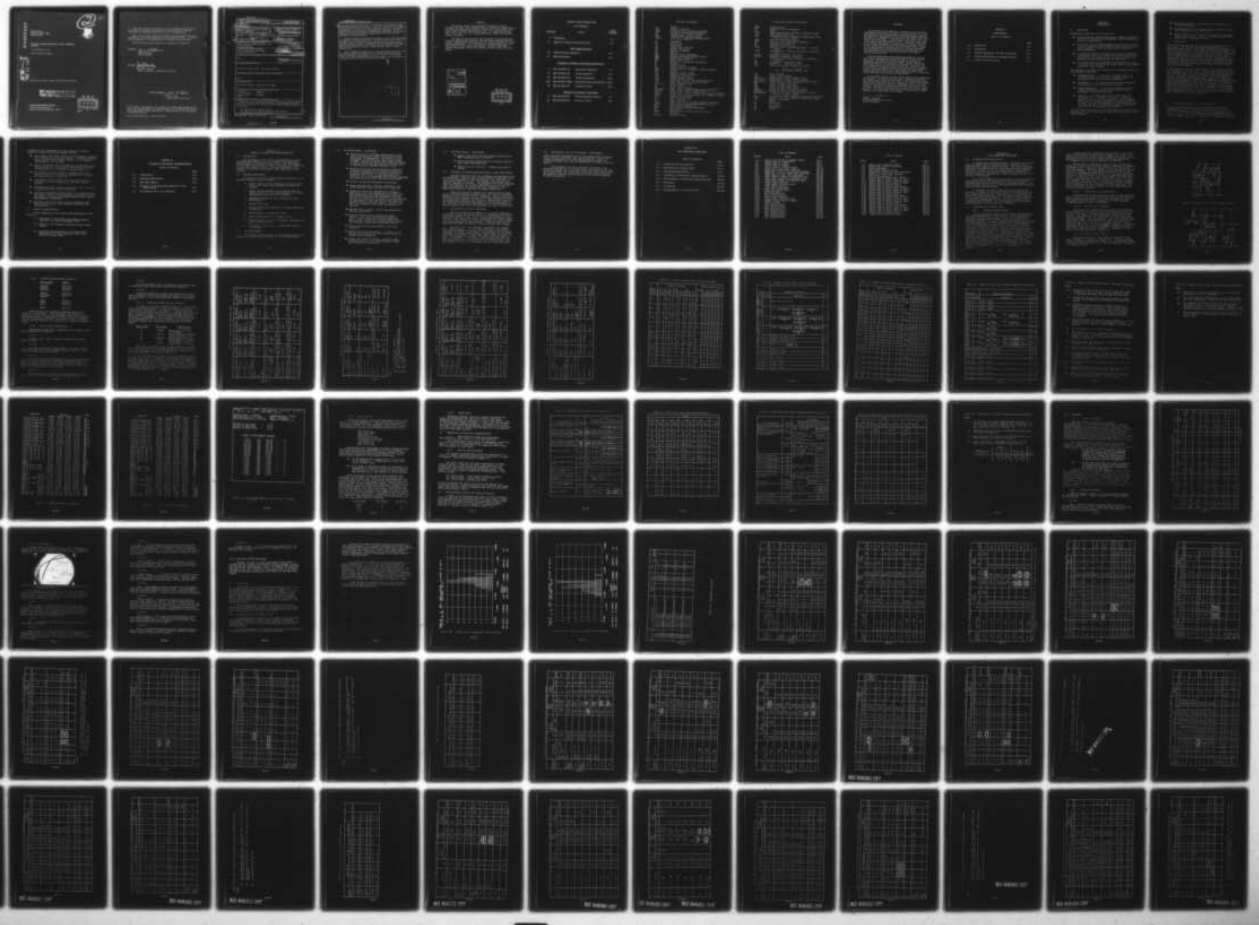

RADC-TR-78-22
Final Technical Report
February 1978

ELECTRICAL CHARACTERIZATION OF LINEAR INTEGRATED CIRCUITS

J.S. Kulpinski, et al

General Electric Company

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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This report covers the work performed by General Electric Ordnance Systems pertaining to the electrical characterization of linear integrated circuits. The period of report is July 1976 to June 1977. The effort was divided into three tasks;

(1) New electrical characterization,
(2) Resolution of problems with existing slash sheets, and
(3) Rewrite of preliminary slash sheets.

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New characterization was performed on five different quad op-amp device types having wide usage in military systems. A slash sheet emanated, once confidence was established in choice of electrical parameters, limits, test circuits and test grouping. Work was begun to characterize quad comparators. The 139 commercial device type was chosen for standardization because of its popularity. Parts were procured and preliminary analysis began. This effort will be completed on a follow-on contract.

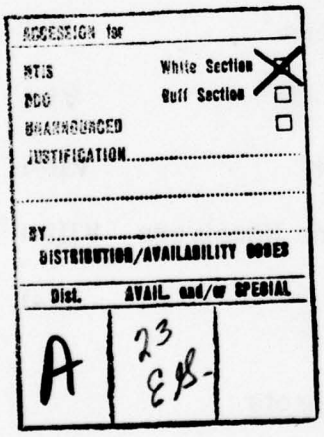
Extensive evaluation and testing was necessary to resolve the problems that was prevalent on existing slash sheets. The slash sheets in question were /101 (Op-Amps), /102 (volt regulators) /103 (comparators), /10404 (line receivers) and /108 (transistor arrays). Users/manufacturers were contacted to isolate problems and parts were procured and tested. Data was analyzed and the slash sheets were revised where necessary to allow qualified sources to produce relevant parts.

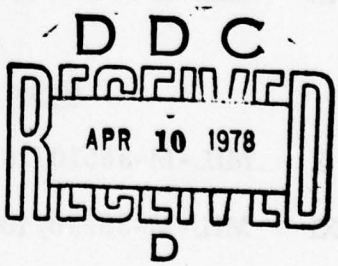
Finally, problems were analyzed for existing slash sheets in much the same way that was applied to preliminary sheets. Lengthy comments submitted by manufacturers and/or users suggested the need for rewrite. After extensive review, /107 (fixed voltage regulators) and /109 (timers) were issued. Details of these efforts will be found in the body of the report.

PREFACE

This Final Report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, New York, under contract F30602-76-C-0345. It covers the period July '76 - July '77. Mr. Thomas Dellecave, RBRM was the RADC Project Engineer.

The work on this project was performed by the Electronic Circuits Engineering Operation and Components Engineering Unit. Project responsibility was held by Mr. John Kulpinski of Circuit Design Engineering. Key individuals who made significant contributions to this report were Messrs. Theodore Simonsen, Richard Paskowsky, Donald Van Alstyne, Herbert Labb, and Jerry Yaple.





LINEAR CHARACTERIZATION

List of Sections

Acronyms and Symbols

A	Ampere
A/D	Analog to Digital
AGED	Advisory Group on Electron Devices
AIA	Aerospace Industries Association
A_{VC}	Voltage gain, collector output
A_{VE}	Voltage gain, emitter output
$A_{VS}(\pm)$	Open loop voltage gain (single-ended. 0 to +, 0 to 5)
BW	Bandwidth
CM	Common mode
cm	Centimeter
CMR	Common mode rejection
CS	Channel Separation
D/A	Digital to Analog
dB	Decibel
DCR	Direct Current Resistance
DESC	Defense Electronics Supply Center
DOD	Department of Defense
DUT	Device Under Test
EIA	Electronic Industries Association
E	Voltage
E_o	Output voltage
GE	General Electric Company
GEOS	General Electric Company, Ordnance Systems
GND	Ground
$+I_{CC}$	Positive supply current
$-I_{CC}$	Negative supply current
ICs	Integrated Circuits
I_{CEX}	Output leakage current
$+I_{IB}$	Input bias current, non-inverting input
$-I_{IB}$	Input bias current, inverting input
I_{I1}, I_{I2}	Input leakage current
I_G	Ground current
I_{IO}	Input offset current
$\Delta I_{IO}/\Delta T$	Input offset current/temperature coefficient
$I_{IO(R)}$	Raised input offset current (/103)
$I_{OS(+)}$	Output short circuit current (for positive output)
$I_{OS(-)}$	Output short circuit current (for negative output)
I_{SCD}	Standby current drain
I_L	Load current (/107)
JAN	Joint Army Navy
JC-41	JEDEC committee on Linear Integrated Circuits
JEDEC	Joint Electron Devices Engineering Council
LSI	Large Scale Integration
LTPD	Lot Tolerance Percent Defectives
mA	Milliampere
MPCAG	Military Parts Control Advisory Group
mV	Millivolt
$N_i(BB)$	Broadband noise

$N_1(PC)$	Popcorn noise
P_D	Quiescent power dissipation
pk	peak
+PSRR	Power Supply Rejection Ratio, positive supply
QPL	Qualified Product List
q/kT	Charge/(Boltzman's constant) (Temperature, °K) q/kT = 25 mV at 25°C
RADC	Rome Air Development Center
SR(+)	Slew rate (max $\triangle V_O/\triangle t$), positive
TA	Ambient temperature
TC	Temperature coefficient
t_{RLHC}	Response time - low-to-high level - collector output
t_{RHLC}	Response time - high-to-low level - collector output
$TR(t_r)$	Transient response, rise time
TR(OS)	Transient response, overshoot
t_s	Settling time of step response to specified accuracy.
TTL	Transistor - transistor logic
T^2L	Transistor - transistor logic
V_{IC}	Input common mode voltage for /10304

$$V_{IC} = -\left[\frac{(+V_{CC}) + (-V_{CC})}{2}\right] + V_{IN}$$

V_{IN}	Input voltage
V_{IO}	Input offset voltage
$V_{IO}(R)$	Raised input offset voltage (/103)
VIO ADJ(+)	Adjustment for input offset voltage
$\triangle V_{IO}/\triangle T$	Input offset voltage temperature coefficient
V_{OL}	Output Voltage, Low Level
V_{OH}	Output Voltage, High Level
V_{OP}	Output voltage swing (peak)
V_{OPP}	Output voltage swing (peak-to-peak)
$V_O(STB)$	Collector output voltage (strobed)
$\triangle V_{TH}/\triangle V_{CL}$	Change in threshold voltage due to change in control voltage (timer).
Z_{is1}	Single-ended input impedance (non-inverting input)
Z_{is2}	Single-ended input impedance (inverting input)
°C	Degrees centigrade
u	Micro
uF	Microfarad
uV	Microvolt
us	Microsecond
$\triangle$	Delta

EVALUATION

The objective of this effort was to characterize specific linear integrated circuits having wide usage in military systems. Electrical test procedures had to be developed and evaluated along with detailed test and burn-in requirements for inclusion in MIL-M-38510 slash sheets. The effort was successful. A new quad op amp slash sheet (/110), containing five device types, has been issued. These device types cover system range of applications from low bias to high speed. Nearly 90% of all military requirements for quad op amps in electronic systems could be achieved by one or more of the listed device types. Because of this specification, system managers who in the past experienced long procurement delays and high specification and materiel costs, will now be able to procure quad op amps quicker, with higher reliability and less cost.

When the program began, many problems associated with existing slash sheets were prevalent limiting the number of sources for each device type. Therefore, much time was devoted to analyzing and recommending specification corrective action. General Electric has done an excellent job in resolving the differences and revising the slash sheets without sacrificing part reliability. Revisions to the op amp (/101E), and comparator (/103B) specifications and an amendment to the line driver/receiver (/104) specification have been issued. Complete rewrites of the positive voltage regulator (/107) and precision timer (/109) specifications were also accomplished.

To aid General Electric in their characterization of quad comparators (LM139 types), a new approach has been taken. Advanced Micro Devices has agreed to test, using their test tapes, recent sampled device types from as many manufacturers that are interested in the MIL-M-38510 program. The test data, even though lacking in completeness, serves as a good reference. That data is compared to GE test data to ascertain if there are tester dissimilarities or anomalies that may lead to false parameter behavior. A follow-on effort will complete the quad comparator characterization and a slash sheet will be issued.

Thomas L Dellecave

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Solid State Applications Section
Reliability Branch

SECTION I

INTRODUCTION

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SECTION I
INTRODUCTION

1.1 Objectives

The specific objectives of this study are:

- To electrically characterize specific linear microcircuit devices for inclusion in MIL-M-38510, "General Specification for Microcircuits"
- To develop test procedures based upon accepted techniques that are compatible with automatic linear testers, which yield consistent results and are least influenced by tester parasitics
- To generate detailed life-test and burn-in circuits and requirements, which will stress the devices beyond that required for most applications, but which will be consistent with the rated capacity of the device
- To prepare detailed MIL-M-38510 slash sheets which will incorporate the results of the above efforts into standard format for final issuance

The development of 38510 specifications is ultimately based upon these general objectives:

- STANDARDIZATION - of devices, packages, tests, to optimize system logistics and to achieve least cost for parts of known quality and reliability
- RELIABILITY - to maintain device/system performance with stress and age in severe environments
- INTERCHANGEABILITY - to achieve repeatable uniform device performance despite lot variations, device redesigns, and multiple sourcing
- QUALITY - to assure that military standards are maintained for a population of devices. There is qualification for generic capability, lot acceptance tests for lot-related parameters, and 100% screening for major and critical parameters; also, there is manufacturer and line certification, process documentation and control, and government surveillance.

The underlying objective of the 38510 program is lower life-cycle system cost. This is achieved by the above objectives in the following ways:

- Device obsolescence is minimized, and redesigns are therefore prevented.
- Documentation and procurement tasks are reduced; therefore, associated costs are reduced.
- Sales volume and multi-sourcing competition will reduce initial device costs. Higher reliability devices will reduce system maintenance costs.

1.2 Background

This effort began in July of 1976, and was completed in a one-year period. At the time that Ordnance Systems began the characterization effort, there was considerable controversy over the status and content of the existing linear slash sheets. The device manufacturers were outspoken about the ills of the specs and the alleged lack of government response to their needs. In order to determine the appropriate course of action, it was necessary to review the history of the spec developments. Each manufacturer was contacted by letter and by telephone and was requested to forward comments on the specs based upon present-time needs. The comments were then arranged in matrix format for study and assessment.

In September of 1976, the manufacturers reactivated the JEDEC JC-41 committee on linear IC's. Some of the manufacturers were very outspoken about the number of parameters required for test and the tight limits on test parameters. Other manufacturers, although similarly discontented, wanted to address specific problems that they were experiencing. Some of the sensitive issues were published in news reports (ELECTRONIC'S BUYERS NEWS, ELECTRONIC ENGINEERING TIMES) which did not put the issues in proper perspective. By the third JC-41 meeting, much of the philosophy concerning the specs was resolved, and the problems with the specific slash sheets were addressed. It took three additional meetings before the bulk of the work on the existing slash sheets was completed to the satisfaction of the government and the majority of the manufacturers.

1.3 General Philosophy for Test Parameters

Test parameters are generally derived from manufacturer's recommendations, from user design parameters, and from the reliability parameters required for quality assurance and conformance. An op amp, for example has many parameters that require testing. "Front end" characteristics such as input bias currents, offset voltage and current, and temperature coefficients

are important to both reliability and design engineers. Further reliability assurance is achieved by screening and operating life "delta" measurements of selected critical parameters.

Other parameters, more significant to the designer, are common mode rejection, power supply rejection, output short-circuit current, output noise, output swing, supply current drain, open-loop gain, slew rate and transient response.

Parameter limits are always a sensitive issue for the maker, since yield is so dependent upon the limits. If two parameters on a chip each have a yield of 80%, the overall yield is 64%. Put two of these chips in a dual package, and the yield drops to 41%; for quads, the net yield becomes 17%. Obviously, with a large number of parameters, yields could get very low even if no single parameter, by itself, has low yield. Since final electrical tests are performed after assembly, there is nothing to be salvaged on the fallout, and these devices (other than catastrophic failures) will most likely become the "38510 processed" or "JAN processed" devices, which in essence are not guaranteed to meet all limits of 38510.

When all is said and done, the selected non-superflous parameters (when successfully tested) will:

- assure higher reliability over a system life-cycle
- constrain the performance of the devices within stated limits
- provide the user with necessary design information.

1.4 General Philosophy for Parameter Limits

When a manufacturer originates a device design and wants to set parameter limits, he takes a careful look at data from pilot runs, adds some room for production-lot variability, and comes up with a data sheet. Another manufacturer decides to produce "the same" part; however, he may first decide to improve upon one or two parameters that might give him a competitive edge. A third maker may enter the marketplace for that device with a design that also meets the original data sheet specs. But unless identical masks and processes are used (not feasible), the device performance cannot be equivalent in all respects. And what about the parameters that aren't on the original data sheet, or are shown only as "typical" characteristics?

Thus evolves the first constraint for the spec writer: set limits that will permit acceptable yields for several sources taking into account manufacturer to manufacturer variability. On the other hand, there are advantages to tight limits. These show up at the user level. A parameter like offset voltage might be set atfive millivolts and find wide application. At four millivolts, it would include perhaps others. So tighter limits lead to wider useage, and fewer device types per system, which leads to easier procurements, less documentation, less system maintenance, and ultimately lower life-cycle cost. Needless to say, the designers' tasks are eased when there is less device variation to account for, and system performance will most likely benefit. The added benefit of consistent device performance minimizes the chance of system problems due to device nonuniformity. Unfortunately, a major penalty accompanies tight limits, and that is device cost. If yields decrease, costs have to increase. Some users argue that tight device limits are not required for their system designs, and that the specs should not penalize the average user because of the needs of a few super users who require superior device characteristics.

In the midst of this controversy is the issue of reliability. Parameters and limits control the device performance, and contribute somewhat to achieving reliability. The other major factors which ensure high reliability are burn-in, quality conformance groups, process qualification and control, and life tests. For life tests. end point limits and deltas for critical reliability parameters are given. Usually, these tests require measurement of certain parameters (such as input offset voltage, input bias current) at room temperature before and after a 1000-hour life test at elevated temperature. The drift which occurs over this life test is given a delta limit, which is often a very small amount. Tester accuracy and repeatability of test measurements influence results and, therefore, mask the true drift somewhat.

For specifications that were already in existence (when GEOS began this study), user impact was a major concern. Changing parameters/limits on significant design parameters would make it necessary for a user to reassess all of his hardware designs in order to determine effects on equipments. Consequently, for devices which had qualified sources for procurement, changes to design parameters were avoided. A prime example of this is the 741 Op Amp, a very popular device for commercial and military equipments. Front-end changes requested by the manufacturers were not recommended since hardwarein the field might be adversely affected.

A summary of the philosophy which has evolved for setting realistic limits for new slash sheets is this:

- The industry data sheet and the JC-41 Committee recommendations are prime sources for limits. A general tightening of limits "until someone hollers" is no longer a philosophy (if it ever was).
- Limits recommended must be justified by sufficient manufacturer data, to be assessed by engineering judgment and supplemented by government-generated data.
- The choice of limits should be consistent with the device technology and with the capabilities of testers and test methods in common use.
- Unnecessarily loose limits, which may introduce non-uniformity or interchangeability problems, must be avoided.
- Unnecessarily tight limits, which permit only one source to become qualified, are not permitted.
- Temperature-dependent parameters will be specified with two sets of limits; one set at 25°C, and another at -55°C and +125°C. The same philosophy holds true for common-mode-dependent parameters.
- Operating life delta limits will be consistent with device technology and test equipment resolution and repeatability.

1.5 Scope of Applied Effort

Three categories of work effort were performed on this contract:

(1) Generation of new detail slash sheets (Quad Op Amps /110, and Quad Comparators /111).

(2) Resolution of problems on existing detail slash sheets.

(3) Rewrites/characterization of proposed detail slash sheets (Voltage Regulators /107, and Precision Timers /109).

SECTION II

APPROACH TO ELECTRICAL CHARACTERIZATION

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SECTION II
APPROACH TO ELECTRICAL CHARACTERIZATION

2.1 Introduction

The approaches to electrical characterization varied, depending upon whether or not the devices were previously characterized on an existing slash sheet. For slash sheet devices which had qualified sources, the impact of change upon the user was a major concern. For new slash sheets, and rewrites of proposed slash sheets, user impact was of less concern.

2.2 Existing Slash Sheets

For devices previously characterized and specified, the approach consists of the following:

* Review history of the development of the original spec to the extent that existing documentation permits.
* Review written comments from manufacturers and users, and solicit up-to-date comments from device manufacturers and the JC-41 Committee.
* Summarize comments in matrix format for study and analysis.
* Obtain device data.
* Perform laboratory evaluation of sample quantities of devices.
* Assess impact of change upon users.
* Make recommendations for changes, if any.
* Review changes with JC-41 Committee, manufacturers, users, and government.
* Incorporate changes into a slash sheet revision or amendment.

2.3 New Slash Sheets

The general approach to new device characterization and generation of slash sheets consists of the following tasks:

2.3 New Slash Sheets - (Continued)

- Assess and select candidate device types, based upon documented user needs and manufacturer and government recommendations. One source of user information is the Military Parts Control Group at DESC. Others are the G12 Solid State EIA Device Committee and the Microelectronics Projects Group of the Electronic Systems Committee of AIA.

- Perform preliminary lab evaluation and analysis of sample quantities of the candidate devices to determine suitability for military applications. Typically this effort is performed using the Tektronix 577 Curve Tracer (with appropriate adapters) and using other standard laboratory instruments.

- Perform reliability assessment and analysis.

- Obtain proposed test circuits, parameters, test conditions and limits from the JC-41 Committee.

- Obtain test data from manufacturer's samples. Typically, 10 or more samples are solicited from each manufacturer via RADC, markings are removed, devices are serialized and identified, and then the group of devices is returned to one manufacturer who has agreed to test and record data using his standard factory automatic tester. Copies of the data are forwarded to all other manufacturers of the part.

- Evaluate test circuits; correct any deficiencies that are identified.

- Develop automatic test capability at GEOS. Typically, the Tektronix S3260 Test System is used. A test program and a device adapter are developed and proofed by correlating data between the automatic tester and a bench test method.

- Procure devices from distributors, for random selection.

- Perform tests and record data. A portion of the manufacturer-supplied devices is also tested to uncover device anomalies.

- Reduce data from all sources. Calculate mean, standard deviation, and minimum/maximum values. Plot histograms of the data.

2.3 New Slash Sheets - (Continued)

- Compare data with published industry data sheets. Make recommendations for limits.
- Review proposed limits with all concerned parties. Make final recommendations.
- Finalize burn-in circuits. Complete the specification.

2.4 Influence of Existing Specifications on New Slash Sheets

Existing specifications are considered an important source of information. However, many of the existing linear specs have been very troublesome to the manufacturers, and repetition of old problems must be avoided. For example, Quad Op Amps are a natural outgrowth of Op Amps. The parameters and test conditions that were developed for Op Amps (38510/101) are, for the most part, applicable to the Quad Op Amp spec (38510/110) with additional parameters required for channel separation.

Other specifications planned for characterization might be in a totally different generic class, and have no precedents. Examples of this are A/D and D/A converters. Even in this case. there are some precedents in many of the specifications previously developed for digital logic devices. Each generic class has its unique characteristics that have to be fully specified in the interests of achieving repeatability and interchangeability. Existing specs often can form a guideline or base to build upon.

2.5 Coordination via JC-41 Committee

The JC-41 Committee on Linear IC's is now an effective organization which has opened the way to organized communication with device manufacturers. Prior to the establishment of this committee, the spec writer had to communicate with manufacturers one at a time. There was little opportunity for candid communication among makers and spec writers. Often one maker did not know what the other was saying or how to request spec changes.

The JC-41 Committee meetings, supplemented by frequent task group meetings, allow for open discussion of problems, proposals for limits, parameters, test circuits, and new device candidates for future slash sheets. The meetings of the parent committee are attended by GEOS, RADC, DESC, and a few users, so that all concerned parties have a voice in decisions that are made. One possible disadvantage of voting ondecisions is that the high-quality maker may be undone by a majority vote. For this reason, GEOS and the government make the final decisions

2.5 Coordination via JC-41 Committee - (Continued)

after objectively assessing all of the comments and recommendations from the committee. The task groups also offer a convenient mechanism for alerting manufacturers to specific problems as they occur, and for requesting a "unified" course of action.

The existence of such a committee, so long as it is properly supported by all manufacturers, takes much of the communication burden off of the spec writer and allows him to spend his contract time more effectively on device characterization. We therefore strongly endorse the role of the JC-41 Committee in 38510 activities.

SECTION III

QUAD OPERATIONAL AMPLIFIERS

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SECTION III
QUAD OPERATIONAL AMPLIFIERS

3.1 Background and Introduction

As large scale integration (LSI) is becoming more commonplace in digital circuit mechanizations, increased circuit densities are coming to linear circuits. User need and vendor capability are instrumental in developing the quad operational amplifier. Because of pin out restrictions, the new quad op amp species do not have offset-voltage-adjust capability or external frequency compensation. Power is common for all four op amps in the package.

In the MIL-M-38510/110 specification for quad operational amplifiers, most of the parameters and test conditions are borrowed from the /101 specifications on single op amps. This also afforded a review of the /101 specification that otherwise would not have been necessary.

In choosing the device types to be specified in the document, a review of vendor spec sheets was conducted and the more promising devices were characterized. In selecting one device over other candidates. the status and market potential of the chosen device is enhanced. In order to be as impartial as possible, recommendations from the joint industry JC-41 Committee were solicited. The JC-41 Committee also provided recommendations on limits and test conditions.

3.2 Descriptions of Device Types

3.2.1 General Characteristics

All quad op amps possess certain common characteristics. The individual amplifiers are similar to single operational amplifiers, except that, because of pin out restrictions, external compensation and offset voltage adjustment are not available options. All have a differential input stage in order to provide high gain for differential signals and much lower gain for common-mode signals. These two inputs are called inverting (-) and non-inverting (+) for their polarity with respect to the output signal. Different techniques are used in the design of these front ends, depending on the electrical parameters to be enhanced. Low input offset voltage, low bias currents, high gain, high input impedance and high common mode rejection are the main desired input characteristics. A level-shifting stage which provides further gain couples the signal to the output. Internal frequency compensation is generally applied to the in-between, level-shifting stage. The output stage almost always is in the form of a complementary emitter follower to provide a single-ended, low-impedance, output signal.

Current limiting is generally incorporated in the output stage so that shorts to ground do not damage the op amp. Protection for shorts to either supply voltage also exists but can not be guaranteed over the full temperature range because the 175°C maximum junction temperature will be exceeded.

Since, from an application point of view, op amps are generally connected with external negative feedback to establish a precision gain, frequency compensation must be applied for stability reasons. Each gain stage of an op amp has an associated break frequency at which the gain rolls off from its DC value. An accompanying phase shift of 45° occurs at the break frequency. This increases to 90° at ten times the break frequency. If the sum of the stage phase shifts equals 180° before the loop gain magnitude has been rolled-off to unity or 0 db, the amplifier will oscillate. An internal frequency compensation capacitor connected across a gain stage provides a Miller effect capacitance to roll the gain off at 20 db/decade. In this way the gain is reduced before the stage phase shifts can render the system unstable.

3.2.2 Unique Device Characteristics

The following devices were chosen early in the characterization effort to be candidate types for the /110 specification. These selections were based on JC-41 recommendations, user anticipated need and enough difference in a major parameter to warrant another device type category.

3.2.2.1 Device type 01 (LM148)

This device is a general purpose op amp with characteristics similar to the /101-01 (741). NPN transistors are used in the input stage. This yields positive polarity input bias current. Its offset voltage specification is worse than its single counterpart (i.e., +6 mV versus +4 mV over the military temperature range, $-55°C \leq T_A \leq 125°C$.) The only parameter where this quad op amp is better than its single counterpart is in supply current (i.e., 4.5 ma for 4 op amps versus 4.2 ma for one op amp at -55°C). Five picofarads of internal compensation capacitance gives the device a specified transient response rise time of one microsecond (maximum). A schematic of one op amp in the device is shown in figure 3-1.

3.2.2.2 Device type 02 (LM149)

The characteristics of this device are identical with type 01 except for frequency compensation. Instead of conventional unity gain compensation, this op amp is compensated for a minimum closed-loop gain of 5. Thus the bandwidth is extended by a factor of five.

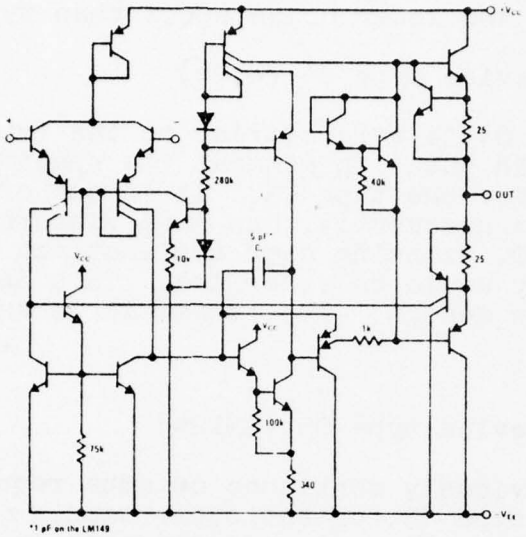


Figure 3-1. Device type 01 and 02 (LM148, LM149)

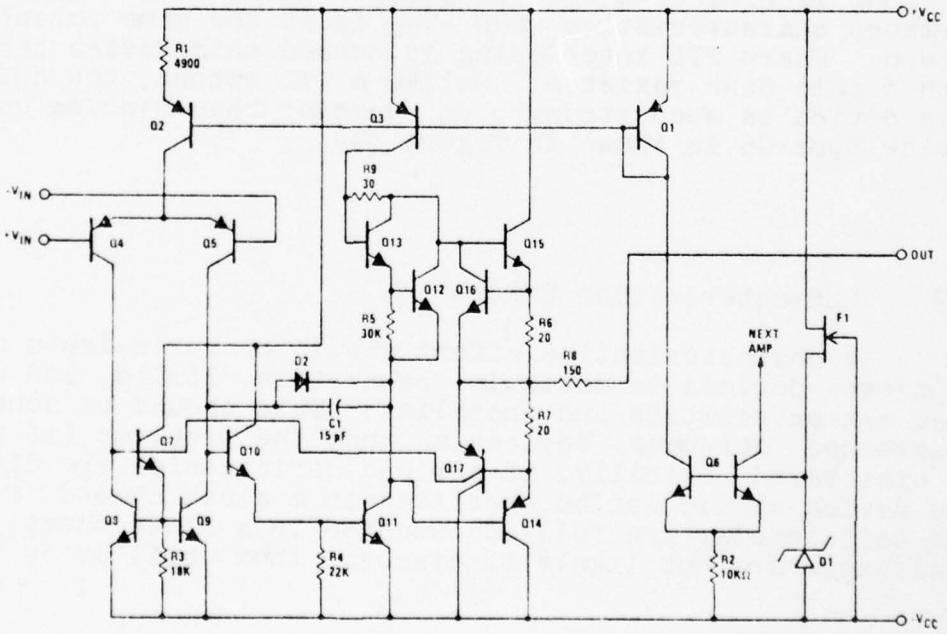


Figure 3-2. Device type 03 (4156/4741)

3.2.2.3 Device type 03 (4156/4741)

Figure 3-2 shows device type 03. It has a PNP differential input and, consequently, negative polarity bias current. At the expense of power supply current, type 03 has a faster transient response and lower noise specs than type 01.

3.2.2.4 Device type 04 (4136)

Device type 04 is very similar to the type 03 except for its non-standard pin out. In general its specifications are more liberal than for the type 03. It is one of the oldest quad op amps and, consequently, has many vendors. By specifying this device in /110, existing user applications are better protected than they would be otherwise. This device is not recommended for new design. The schematic is shown in figure 3-3.

3.2.2.5 Device type 05 (LM124)

All the previously mentioned op amps require dual power supplies. Device type 05, on the other hand, is meant to operate from a single supply. Its main advantage is in low power and single power supply applications. The input stage is designed with PNP transistors thus permitting the common mode range to include ground. The output stage has a 50 uA pull-down current source so that it can swing to ground for light loads. Compared to the other quad op amps in the /110 family, the type 05 has the most liberal specifications since there is a decrease in performance characteristics when $-V_{CC}$ is at the same potential as ground. Where TTL interfacing is needed this device can be used with a pull-down resistor. Unlike a TTL output, the output of this device is much stronger on sourcing than sinking current. Device type 05 is shown in figure 3-4.

3.3 Characterization Effort

A characterization effort should be an in-depth study of candidate devices to determine parameters, limits, and unspecified characteristics and anomalies. This should be done on unscreened mil-temp devices so that the problems (if any) can be discovered. Finally, if serious deficiencies are discovered, the device should not be specified in a slash sheet. Even if the deficiencies are fully documented in a slash sheet, potential users are not likely to discover them until it is too late.

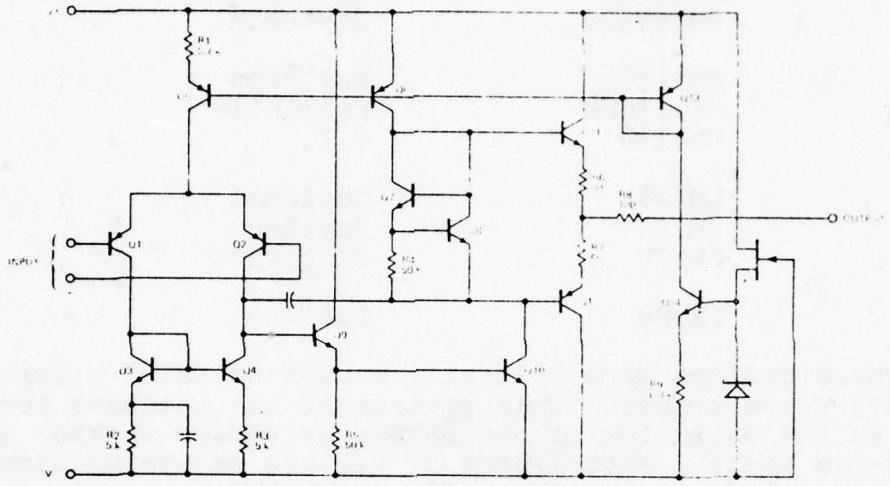


Figure 3-3. Device type 04 (4136)

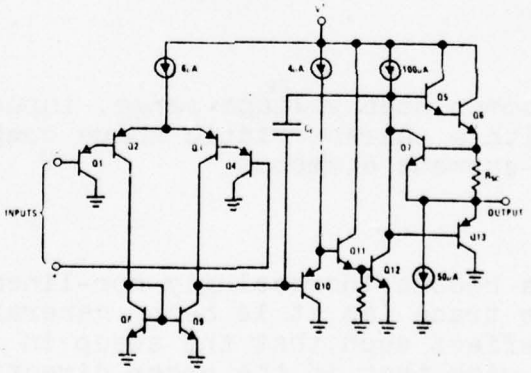


Figure 3-4. Device type 05 (LM124)

3.3.1 Initial Characterization Devices

Device Type	Vendor
uA3503D	Fairchild
MC3503	Motorola
RM3503DC	Raytheon
RM4136	Raytheon
uA4136DM	Fairchild
RM4136	T.I.
LM124	National
LM124	Raytheon
LM124	Signetics
LM148	National

These devices were initially evaluated using a Tektronix 577 curve tracer. This instrument was adequate for looking at the variation of one parameter versus another on a small sample basis. Photographs of various parameter displays are shown in the data section. Since the 577 has a storage screen, several families of curves could be observed simultaneously.

3.3.2 Curve Tracer Observations

Same general observations resulting from a review of the oscillographs are as follows:

3.3.2.1

In some cases, offset voltage increases with reduced supply voltage.

3.3.2.2

Over the common mode voltage range, input bias current varies directly with a characteristic shape composed of resistive and constant-current elements.

3.3.2.3

Gain curves become increasingly non-linear with increased loading. Also the trace (as it is being generated) tends to have a hystersis effect such that the sweep in one direction does not coincide with that in the other direction unless the sweep rate is slowed down considerably.

3.3.2.4

The LM124, when used with dual supplies, has a significant deadband "spike" in its voltage gain characteristic.

3.3.2.5

The characteristic gain non-linearity of a device type is repetitive with like devices almost as a signature.

3.3.2.6

Quantative values for common mode rejection and power supply rejection can be calculated from points on the curves, but this method is very time consuming compared to automatic methods.

3.3.3 Tektronix S-3260 Automatic Testing

In order to accumulate sufficient data for characterization in a reasonable amount of time, automatic test methods would have to be employed. To this end, a test program was written for a Tektronix S-3260 tester. A special interface card was built. Before taking the data on the available devices at RADC, a survey was made of all known quad op amps and their parameters. This chart is shown in table 3-1. From this chart and recommendations of the JC-41 Committee, the following candidate devices were tentatively selected as /110 device types.

Device Type	Comm. Type	Description
01	LM148	Medium Power 741 Type Performance
02	LM149	Under Compensated (Medium Speed) Version of 01
03	4741/4156	Medium Speed, Low Noise
04	4136	Medium Speed. Low Noise (Alternate Pin Out)
05	LM124	Single Supply, Low Power

The S-3260 test fixture and the MIL-M-38510/110 static test circuit were developed simultaneously as shown in figure 3-5. How this test circuit and the S-3260 are configured for the various parameters is shown in table 3-2.

A typical data output sheet on a single device is shown in table 3-3. The time required to take these measurements over the temperature range and print out the results was under four minutes. The data was also logged into file so that a statistical analysis of the data could be performed. Table 3-4 shows a typical statistical summary of offset voltage V_{IO} for a single condition of common mode voltage (-15V) and temperature (-55°C) on 14 LM148 quad op amps (56 op amps).

Table 3-1. Quad op amp comparison chart

Parameter	LM148	LM149	uA3503	RM3503A	uA4136
V_{IO} @ 25°C @ -55/125°C	**5 mV #**6 mV	**5 mV **6 mV	**5 mV **6 mV	**4 mV **6 mV	**5 mV **6 mV
I_{IO} @ 25°C @ -55/125°C	**25 nA #**75 nA	**25 nA **75 nA	**50 nA **200 nA	**50 nA **200 nA	**200 nA **500 nA
$\pm I_{IB}$ @ 25°C @ -55/125°C	**100 nA #**325 nA	**100 nA **325 nA	**500 nA **1500 nA	**400 nA **1500 nA	**500 nA **1500 nA
$\pm$PSRR	#77 dB	77 dB	150 uV/V	50 uV/V	150 uV/V
CMR	70 dB	70 dB	70 dB	70 dB	70 dB
N_1(BB)					
I_{CC} @ 25°C @ N.L.	#**3.6 mA	**3.6 mA	**4 mA	**4 mA	***7 mA
V_{OP} @ 10 K @ +15V	+12V	+12V	+12V		+12V
@ 2 K @ $\pm$15V	$\pm$10V	$\pm$10V	$\pm$10V	$\pm$13V	$\pm$10V
A_{VS} @ 2 K	50 V/mV 7/	20 V/mV	25 V/mV	25 V/mV	25 V/mV
t_r (risetime)	#**1 uS	**250 nS	*.3 uS		*.13 uS
OS (overshoot)	#**30%		*20%		*5%
$\pm$SR (slew rate)	#.2 V/uS	.8 V/uS	*.6 V/uS	*1.2 V/uS	1.3 V/uS
CS (channel sep.)	*120 dB	*120 dB	*120 dB		*105 dB
BW (unity gain)	*1 MHz	*4 MHz 5/	*1 MHz	*1 MHz	*3 MHz
Crossover Distortion	No	No	*1%	*1%	No

Table 3-1. Quad op amp comparison chart (Continued)

Parameter	LM148	LM149	uA3503	RM3503A	uA4136
Std. Pin-Out	Yes	Yes	Yes	Yes	No
$\pm V_{CC}$ (max)			**$\pm$18V	**$\pm$18V	**$\pm$22V
Quad 741 type	Yes	Yes	?	Yes ?	Yes
Single Supply Type	No	No	Yes	Yes	No
PNP/NPN Input	NPN	NPN	PNP	PNP	PNP
Output Current Limit	Yes	Yes	$I_{OS}(+)$ Only	$I_{OS}(+)$ Only	Yes
Vendor	National	National	Fairchild	Raytheon	Fairchild
Data Source	IC Master '77		Fairchild	Raytheon	Fairchild
Comments	Quad 741	3/	Single Supply	High Slew Rate	Low Noise

NOTES:

1/ L. Goldstein, Nat. inputs #.
2/ Typical values *.
3/ Wide band, under-compensated op amp.
4/ ** = Maximum values; unmarked values are minimums.
5/ BW @ Av $\geq$ 5.
6/ Low noise and high slew rate.
7/ $T_A = 25^{\circ}C$

Table 3-1. Quad op amp comparison chart

Parameter	RM4156	HA-4741-2	HA-4602-2	LM124	LM124A	MC3571
V_{IO} @ 25°C @ -55/125°C	**3 mV **5 mV	**3 mV **5 mV	**2.5 mV **3 mV	**5 mV **7 mV	**2 mV **4 mV	6 mV
I_{IO} @ 25°C @ -55/125°C	**30 nA **75 nA	**30 nA **75 nA	**75 nA **125 nA	**30 nA **100 nA	**10 nA **30 nA	.05 nA
$\pm I_{IB}$ @ 25°C @ -55/125°C	**200 nA **325 nA	**200 nA **325 nA	**200 nA **325 nA	**150 nA **300 nA	**50 nA **100 nA	0.5 nA
$\pm$ PSRR	80 dB	80 dB	86 dB	65 dB	65 dB	
CMR	80 dB	80 dB	86 dB	70 dB	70 dB	70 dB
N_1(BB)	**2 uVrms	*9nV/VHz	*8nV/VHz			
I_{CC} @ 25°C @ N.L.	5 mA	5 mA	4.6 mA	3 mA	3 mA	
V_{OP} @ 10 K @ +15V @ 2 K @ $\pm$15V	+12V $\pm$10V	+12V $\pm$10V	+12V $\pm$10V	+13.5V $\pm$13V		
A_{VS} @ 2 K	25 V/mV	25 V/mV	100 V/mV	25 V/mV	50 V/mV 7/	50 V/mV 7/
t_r (rise time)	*50 nS	*75 nS	*50 nS			
OS (over shoot)	*25%	*25%	*30%			
$\pm$SR (slew rate)	1.3 V/uS	*1.6 V/uS	*4 V/uS			20 V/uS
CS (channel rate)	*108 dB	*108 dB				
BW (unity gain)	2.8 MHz	*3.5 MHz	*8 MHz		*1 MHz	10 MHz
Crossover Distortion	No	No	No	Yes	Yes	

Table 3-1. Quad op amp comparison chart (Continued)

Parameter	RM4156	HA-4741-2	HA-4602-2	LM124	LM124A	MC3571
Std. Pin-Out	Yes	Yes	Yes	Yes	Yes	
$\pm V_{CC}$ (max)	**±20V	**±20V	**±20V	#**±18V		
Quad 741 Type	Yes	Yes	Yes	No	No	
Single Supply Type	No	No	No	Yes	Yes	
PNP/NPN Input	PNP	PNP	PNP/NPN	PNP	PNP	
Output Current Limit	Yes	Yes	Yes	I_{OS}(+) Only		
Vendor	Raytheon	Raytheon	Harris	National	National	Motorola
Data Source	Raytheon	Raytheon	Harris	National	IC Master '77	IC Master '77
Comments	6/	6/	6/	Single Supply	Low Power	FET, Wideband

Table 3-2. Table of static test circuit conditions

Parameter Symbol	Applied Voltages -01, 02, 03, 04			-05			Notes	Relay States 6/ (1=ON, 0=OFF)					
	$+V_{CC}$	$-V_{CC}$	V_A	$+V_{CC}$	$-V_{CC}$	V_A		K_5	K_6	K_7	K_8	K_9	K_{10}
V_{IO}	35	-5	-15	30	0	-15	1/	0	0	0	0	0	0
	5	-35	15	2	-28	15		0	0	0	0	0	0
	20	-20	0	30	0	-1.4		0	0	0	0	0	0
	5	-5	0	5	0	-1.4		0	0	0	0	0	0
I_{IO}	35	-5	-15	30	0	-15	5/	1	1	0	0	0	0
	5	-35	15	2	-28	15		1	1	0	0	0	0
	20	-20	0	30	0	-1.4		1	1	0	0	0	0
	5	-5	0	5	0	-1.4		1	1	0	0	0	0
$+I_{IB}$	35	-5	-15	30	0	-15	3/	1	0	0	0	0	0
	5	-35	15	2	-28	15		1	0	0	0	0	0
	20	-20	0	30	0	-1.4		1	0	0	0	0	0
	5	-5	0	5	0	-1.4		1	0	0	0	0	0
$-I_{IB}$	35	-5	-15	30	0	-15	3/	0	1	0	0	0	0
	5	-35	15	2	-28	15		0	1	0	0	0	0
	20	-20	0	30	0	-1.4		0	1	0	0	0	0
	5	-5	0	5	0	-1.4		0	1	0	0	0	0
+PSRR	10	-20	0	20	0	-1.4		0	0	0	0	0	0
-PSRR	20	-10	0	-	-	-		0	0	0	0	0	0
CMR	35	-5	-15	30	0	-15	2/	0	0	0	0	0	0
	5	-35	15	2	-28	15		0	0	0	0	0	0
$I_{OS(+)}$	15	-15	-10	30	0	-25	7/	0	0	0	0	1	0
$I_{OS(-)}$	15	-15	10	-	-	-	7/	0	0	0	0	1	0
I_{CC}	15	-15	0	30	0	-15		0	0	0	0	0	0
$+V_{OP}$	20	-20	-20	20	0	-30	R_L = 10 KΩ	0	0	0	1	0	0
$-V_{OP}$	20	-20	20	-	-	-		0	0	0	1	0	0
V_{OP}	-	-	-	5	0	-5		0	0	0	1	0	0

Table 3-2. Table of static test circuit conditions

Measure		Measured Parameter	
Value	Units	Equation	Units
E_1 E_2 E_3 E_4	V	$V_{IO} = E_1,\ E_2,\ E_3,\ E_4$	mV
E_5 E_6 E_7 E_8	V	$I_{IO} = \frac{(E_1-E_5)\times10^6}{R_S},\ \frac{(E_2-E_6)\times10^6}{R_S},\ \frac{(E_3-E_7)\times10^6}{R_S},\ \frac{(E_4-E_8)\times10^6}{R_S}$	nA
E_9 E_{10} E_{11} E_{12}	V	$+I_{IB} = \frac{(E_1-E_9)\times10^6}{R_S},\ \frac{(E_2-E_{10})\times10^6}{R_S},\ \frac{(E_3-E_{11})\times10^6}{R_S},\ \frac{(E_4-E_{12})\times10^6}{R_S}$	nA
E_{13} E_{14} E_{15} E_{16}	V	$-I_{IB} = \frac{(E_{13}-E_1)\times10^6}{R_S},\ \frac{(E_{14}-E_2)\times10^6}{R_S},\ \frac{(E_{15}-E_3)\times10^6}{R_S},\ \frac{(E_{16}-E_4)\times10^6}{R_S}$	nA nA
E_{17}	V	$+PSRR = (E_3-E_{17}) \times 100$	uV/V
E_{18}	V	$-PSRR = (E_3-E_{18}) \times 100$	uV/V
E_1 E_2	V	$CMR = 20 \log \left\lvert \frac{30000}{E_1-E_2} \right\rvert$	dB
I_{OS1}	mA	$I_{OS(+)} = I_{OS1}$	mA
I_{OS2}	mA	$I_{OS(-)} = I_{OS2}$	mA
I_{CC}	mA	$I_{CC} = I_{CC}$	
$(E_O)_1$	V	$+V_{OP} = (E_O)_1$	V
$(E_O)_2$	V	$-V_{OP} = (E_O)_2$	V
$(E_O)_3$	V	$+V_{OP} = (E_O)_3$	V

Table 3-2. Table of static test circuit conditions (Continued)

Parameter Symbol	Applied Voltages -01, 02, 03, 04			-05			Notes	Relay States 6/ (1=ON, 0=OFF)					
	$+V_{CC}$	$-V_{CC}$	V_A	$+V_{CC}$	$-V_{CC}$	V_A		K_5	K_6	K_7	K_8	K_9	K_{10}
$+V_{OP}$	20	-20	-20	30	0	-30	R_L= 2KΩ	0	0	1	0	0	0
$-V_{OP}$	20	-20	20	-	-	-		0	0	1	0	0	0
$+V_{OP}$	-	-	-	5	0	-5		0	0	1	0	0	0
$A_{VS}(+)$	20	-20	-15	-	-	-	R_L= 10KΩ	0	0	0	1	0	0
$A_{VS}(-)$	20	-20	15	-	-	-		0	0	0	1	0	0
$A_{VS}(+)$	20	-20	-15	-	-	-	R_L= 2KΩ	0	0	1	0	0	0
$A_{VS}(-)$	20	-20	15	-	-	-		0	0	1	0	0	0
$A_{VS}(+)$	-	-	-	30	0	-26	R_L= 10KΩ	0	0	0	1	0	0
	-	-	-	30	0	-1		0	0	0	1	0	0
$A_{VS}(+)$	-	-	-	30	0	-16	R_L= 2KΩ	0	0	1	0	0	0
	-	-	-	30	0	-1		0	0	1	0	0	0
A_{VS}	5	-5	-2	5	0	-3	R_L= 10KΩ	0	0	0	1	0	0
	5	-5	2	5	0	-1		0	0	0	1	0	0
A_{VS}	5	-5	-2	5	0	-3	R_L= 2KΩ	0	0	0	0	0	0
	5	-5	2	5	0	-1		0	0	0	0	0	0
$N_1(BB)$	20	-20	0	30	0	0		0	0	0	0	0	1
$N_1(PC)$	20	-20	0	30	0	0	12/	1	1	0	0	0	1
V_{OL}	-	-	-	30	0	30	R_L= 10KΩ	0	0	0	1	0	0
V_{OH}	-	-	-	30	0	-30	I_{OH}= 10mA	0	0	0	0	0	0
V_{OL}	-	-	-	30	0	30	I_{OL}= 5mA	0	0	0	0	0	0
V_{OH}	-	-	-	4.5	0	-5	I_{OH}= 10mA	0	0	0	0	0	0
V_{OL}	-	-	-	4.5	0	5	I_{OL}= 8uA	0	0	0	0	0	0

Table 3-2. Table of static test circuit conditions (Continued)

Measure		Measured Parameter			
Value	Units	Equation			Units
$(E_O)_4$	V	$+V_{OP} = (E_O)_4$			V
$(EO)_5$	V	$-V_{OP} = (E_O)_5$			V
$(E_O)_6$	V	$+V_{OP} = (E_O)_6$			V
E_{19} / E_{20}	V	$+A_{VS} = \frac{15}{E_3 - E_{19}}$ $-A_{VS} = \frac{15}{E_{20} - E_3}$ 9/			V/mV
E_{21} / E_{22}	V	$+A_{VS} = \frac{15}{E_3 - E_{21}}$ $-A_{VS} = \frac{15}{E_{22} - E_3}$			V/mV
E_{23} E_{24}	V	$A_{VS} = \frac{25}{E_{24} - E_{23}}$			V/mV
E_{25} E_{26}	V	$A_{VS} = \frac{15}{E_{26} - E_{25}}$			V/mV
E_{27} E_{28}	V	$A_{VS} = \frac{V_A}{E_{28} - E_{27}}$	01 - 04	$\triangle V_A = 4$	V/mV
			05	$\triangle V_A = 2$	
E_{29} E_{30}	V	$A_{VS} = \frac{V_A}{E_{30} - E_{29}}$	01 - 04	$\triangle V_A = 4$	V/mV
			05	$\triangle V_A = 2$	
$(E_O)_7$	mVrms	$N_1(BB) = (E_O)_7/1000$			uVrms
$(E_O)_8$	mVpk	$N_1(PC) = (E_O)_8/1000$			uVpk
$(E_O)_9$	mV	$V_{OL} = (E_O)_9$			mV
$(E_O)_{10}$	V	$V_{OH} = (E_O)_{10}$			V
$(E_O)_{11}$	V	$V_{OL} = (E_O)_{11}$			V
$(EO)_{12}$	V	$V_{OH} = (E_O)_{12}$			V
$(E_O)_{13}$	V	$V_{OL} = (E_O)_{13}$			V

Table 3-2. Table of static test circuit conditions (Continued)

NOTES:

1/ Selection of the op amp under test is made with relay contacts K_1, K_2, K_3 and K_4. Use the parameter table to determine the relay contact states for each test.

2/ Common mode rejection is calculated using the offset voltage values measured at the common mode range end points.

3/ Stabilizing capacitors may be added as required if needed to prevent oscillation. Also, proper wiring procedures shall be followed to prevent oscillation. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.

4/ Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of switch positions (e.g. disable voltage supplies, current limit etc.).

5/ R_S = 20 KΩ for -01, 02, 03, 04 and 05.

6/ The relays are shown to indicate circuit test connections only. They are not required for the actual test mechanization. 1 and 0 refer to the energized and de-energized states of the relays.

7/ Only one op amp at a time shall be tested with a short to ground for t $\leq$ 25 ms.

8/ Any oscillation greater than 300 mV in amplitude (pk-pk) shall be cause for device failure.

9/ To minimize thermal drift, the reference voltage for gain measurement E_3 shall be taken immediately prior to or after the reading corresponding to device gain (E_{21}, E_{22}, E_{23} and E_{24}).

10/ All resistors are $\pm$0.1% tolerance, capacitors are $\pm$10% tolerance.

11/ Adequate settling time shall be allowed such that each parameter has settled to 5% of its final value.

12/ Popcorn noise $(E_O)_8$ shall be measured for 15 seconds. Broadband noise $(E_O)_7$ shall be measured with an RMS voltmeter with a bandwidth of 10 Hz to 5 KHz.

Table 3-2. Table of static test circuit conditions (Continued)

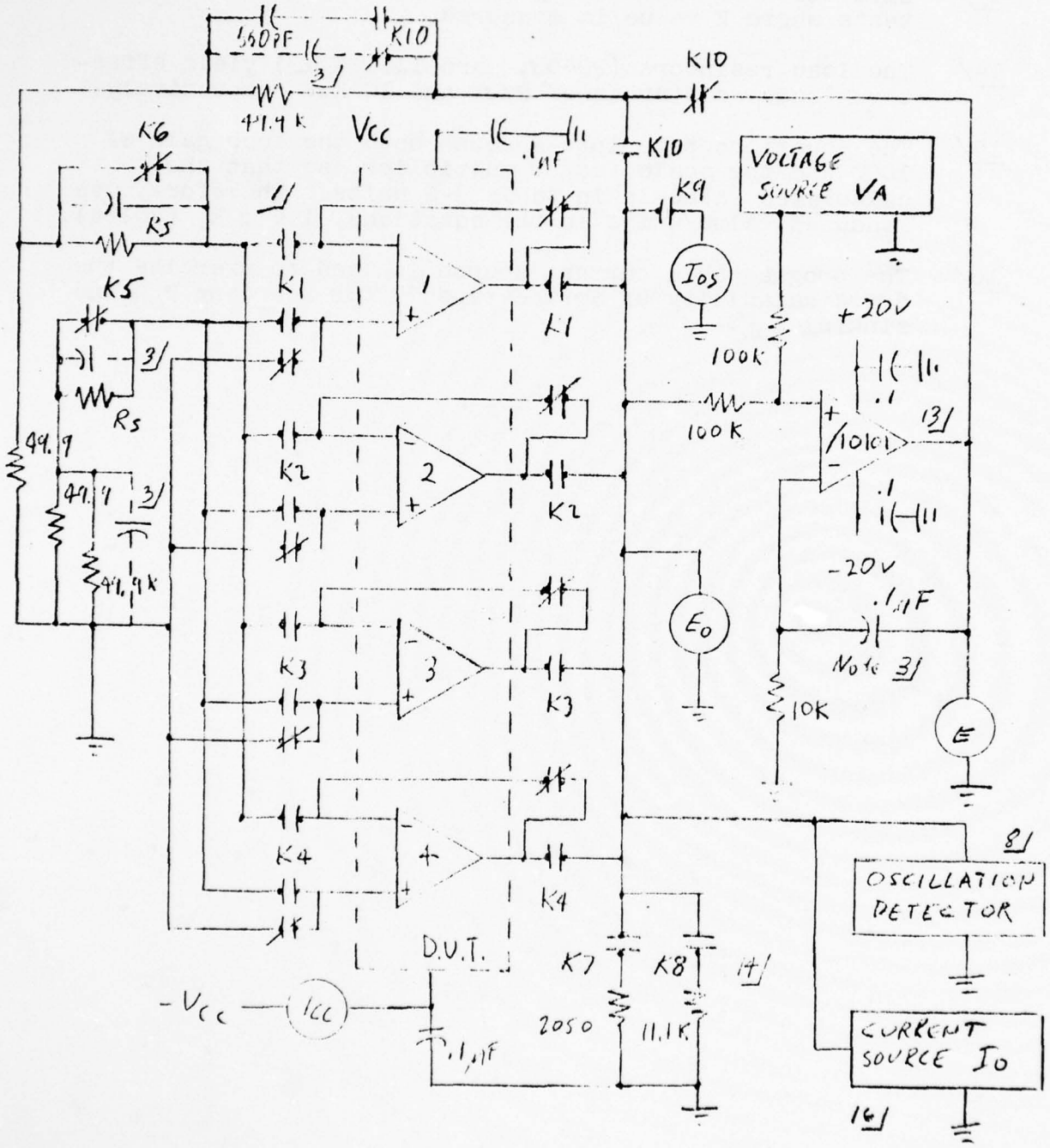
NOTES:

13/ Saturation of the nulling amplifier is not allowed on tests where E value is measured.

14/ The load resistors (2040Ω and 11.1 KΩ) yield effective load resistances of 2KΩ and 10 KΩ respectively.

15/ The equations take into account both the loop gain of 1000 and the scale factor multiplier, so that the calculated value is in table 3-2 units. Therefore, use measured value/units in the equations, i.e., E_1 (volts).

16/ The programmable current source is used to exercise the drive capability of device type 05 for sourcing I_{OH} and sinking I_{OL}.



Notes are given after table 3-2.

Figure 3-5. Test circuit for static tests

DEVICE TYPE: 148 ; S/N: 10 ; DATE CODE: 7631

PARAMETER	25 DEG C				UNITS
	OPAMP1	OPAMP2	OPAMP3	OPAMP4	
VIO AT 35, -5,-15	1.520	-530.0M	900.0M	1.455	MV
D-VIO/D-T FROM 25 OC					UV/OC
VIO AT 5,-35, 15	1.395	-800.5M	705.0M	1.295	MV
D-VIO/D-T FROM 25 OC					UV/OC
VIO AT 20,-20, 0	1.435	-706.5M	780.0M	1.360	MV
D-VIO/D-T FROM 25 OC					UV/OC
VIO AT 5, -5, 0	815.0M	-1.175	104.5M	800.0M	MV
D-VIO/D-T FROM 25 OC					UV/OC
IIO AT 35, -5,-15	-2.000	-1.875	-2.500	-2.000	NA
D-IIO/D-T FROM 25 OC					PA/OC
IIO AT 5,-35, 15	-2.500	-2.125	-2.000	-2.250	NA
D-IIO/D-T FROM 25 OC					PA/OC
IIO AT 20,-20, 0	-3.000	-1.800	-2.500	-2.250	NA
D-IIO/D-T FROM 25 OC					PA/OC
IIO AT 5, -5, 0	-3.000	-1.000	-1.575	-2.250	NA
D-IIO/D-T FROM 25 OC					PA/OC
IIB(+) AT 35, -5,-15	-6.000	-5.350	-5.500	-5.750	NA
IIB(+) AT 5,-35, 15	21.25	21.22	21.62	21.00	NA
IIB(+) AT 20,-20, 0	16.25	16.92	17.25	16.75	NA
IIB(+) AT 5, -5, 0	11.60	13.50	12.00	11.60	NA
IIB(-) AT 35, -5,-15	-3.750	-3.525	-2.250	-3.500	NA
IIB(-) AT 5,-35, 15	24.00	24.60	24.00	23.50	NA
IIB(-) AT 20,-20, 0	20.00	19.65	19.50	19.50	NA
IIB(-) AT 5, -5, 0	13.50	13.00	13.65	13.00	NA
PSRR(+)	37.50	35.85	43.80	39.50	UV/V
PSRR(-)	35.00	28.85	39.35	34.00	UV/V
CMR AT VCM = +-15V	107.6	100.9	103.7	105.5	DB
ICC AT VCC = +-20V	-2.465	-2.455	-2.450	-2.450	MA
ICC AT VCC = +-15V	-2.245	-2.240	-2.235	-2.230	MA
IOS(+)	-28.55	-28.95	-29.10	-28.80	MA
IOS(-)	18.95	19.10	18.80	18.60	MA
VOPP(+) RL=10K	19.15	19.15	19.15	19.15	V
VOPP(-) RL=10K	-17.55	-17.55	-17.55	-17.55	V
VOPP VLT SWING RL=10K	36.70	36.70	36.70	36.70	V
VOPP(+) RL=2K	17.75	17.75	17.75	17.75	V
VOPP(-) RL=2K	-16.70	-16.65	-16.70	-16.75	V
VOPP VLT SWING RL=2K	34.45	34.40	34.45	34.50	V
AVS(+) RL=10K	-71.43	-90.63	-90.91	-73.17	V/MV
AVS(+) RL=2K	-75.00	-94.94	-88.24	-78.95	V/MV
AVS(-) RL=10K	-500.0	-535.7	-428.6	-750.0	V/MV
AVS(-) RL=2K	-428.6	-352.9	-375.0	-600.0	V/MV
AVS AT +-5V RL=10K	910.1M	863.0M	1.030	920.6M	V/MV
AVS AT +-5V RL=2K	809.7M	770.7M	888.2M	817.2M	V/MV

Table 3-3. LM148 data sheet

PARAMETER		-55 DEG C				UNITS
		OPAMP1	OPAMP2	OPAMP3	OPAMP4	
VIO AT 35, -5, -15		2.125	389.0M	1.870	2.625	MV
D-VIO/D-T FROM 25 OC		-7.563	-11.49	-12.13	-14.63	UV/OC
VIO AT 5, -35, 15		1.755	-82.50M	1.410	2.075	MV
D-VIO/D-T FROM 25 OC		-4.500	-8.975	-8.813	-9.750	UV/OC
VIO AT 20, -20, 0		1.915	67.50M	1.570	2.275	MV
D-VIO/D-T FROM 25 OC		-6.000	-9.675	-9.875	-11.44	UV/OC
VIO AT 5, -5, 0		-300.5M	-1.820	-424.5M	855.0M	MV
D-VIO/D-T FROM 25 OC		13.94	8.063	6.613	-687.5M	UV/OC
IIO AT 35, -5, -15		-2.500	225.0M	-1.750	-1.500	NA
D-IIO/D-T FROM 25 OC		6.250	-26.25	-9.375	-6.250	PA/OC
IIO AT 5, -35, 15		-4.500	-775.0M	-4.500	-4.750	NA
D-IIO/D-T FROM 25 OC		25.00	-16.88	31.25	31.25	PA/OC
IIO AT 20, -20, 0		-3.000	-1.800	-4.500	-4.750	NA
D-IIO/D-T FROM 25 OC		-74.51U	-4.470U	25.00	31.25	PA/OC
IIO AT 5, -5, 0		-3.225	750.0M	-3.275	-4.000	NA
D-IIO/D-T FROM 25 OC		2.812	-21.87	21.25	21.88	PA/OC
IIB(+) AT 35, -5, -15		-13.25	-10.65	-11.25	-12.00	NA
IIB(+) AT 5, -35, 15		34.25	37.55	35.75	34.25	NA
IIB(+) AT 20, -20, 0		28.00	29.43	28.50	27.25	NA
IIB(+) AT 5, -5, 0		20.33	23.75	20.60	18.02	NA
IIB(-) AT 35, -5, -15		-11.50	-12.18	-9.750	-12.00	NA
IIB(-) AT 5, -35, 15		38.75	38.38	40.25	39.75	NA
IIB(-) AT 20, -20, 0		30.50	31.60	33.25	32.50	NA
IIB(-) AT 5, -5, 0		22.65	21.50	24.38	24.25	NA
PSRR(+)		136.7	122.7	127.2	115.5	UV/V
PSRR(-)		135.5	118.8	123.7	109.5	UV/V
CMR AT VCM = +-15V		98.18	96.07	96.29	94.74	DB
ICC AT VCC = +-20V		-3.305	-3.300	-3.300	-3.300	MA
ICC AT VCC = +-15V		-3.025	-3.020	-3.015	-3.015	MA
IOS(+)		-31.65	-34.00	-35.30	-34.00	MA
IOS(-)		28.60	29.10	28.75	28.40	MA
VOPP(+)	RL=10K	19.05	19.05	19.05	19.00	V
VOPP(-)	RL=10K	-17.10	-17.05	-17.05	-17.10	V
VOPP VLT SWING	RL=10K	36.15	36.10	36.10	36.10	V
VOPP(+)	RL=2K	17.75	17.75	17.75	17.75	V
VOPP(-)	RL=2K	-16.50	-16.45	-16.50	-16.50	V
VOPP VLT SWING	RL=2K	34.25	34.20	34.25	34.25	V
AVS(+)	RL=10K	-24.39	-29.59	-27.78	-23.44	V/MV
AVS(+)	RL=2K	-25.42	-29.89	-28.04	-24.39	V/MV
AVS(-)	RL=10K	-200.0	-247.1	-200.0	-187.5	V/MV
AVS(-)	RL=2K	-166.7	-230.1	-230.8	-176.5	V/MV
AVS AT +-5V	RL=10K	614.8M	579.7M	610.8M	609.8M	V/MV
AVS AT +-5V	RL=2K	580.8M	548.3M	578.7M	581.4M	V/MV

Table 3-3. LM148 data sheet (Continued)

PARAMETER		125 DEG C				UNITS
		OPAMP1	OPAMP2	OPAMP3	OPAMP4	
VIO AT 35, -5,-15		1.985	-655.0M	1.045	1.890	MV
D-VIO/D-T FROM 25 OC		4.650	-1.250	1.450	4.350	UV/OC
VIO AT 5,-35, 15		1.805	-983.0M	785.0M	1.690	MV
D-VIO/D-T FROM 25 OC		4.100	-1.825	800.0M	3.950	UV/OC
VIO AT 20,-20, 0		1.875	-865.0M	880.0M	1.775	MV
D-VIO/D-T FROM 25 OC		4.400	-1.585	1.000	4.150	UV/OC
VIO AT 5, -5, 0		2.290	-365.5M	1.140	2.235	MV
D-VIO/D-T FROM 25 OC		14.75	8.095	10.55	14.35	UV/OC
IIO AT 35, -5,-15		1.500	1.250	2.500	2.250	NA
D-IIO/D-T FROM 25 OC		35.00	31.25	50.00	42.50	PA/OC
IIO AT 5,-35, 15		0.000	675.0M	1.250	500.0M	NA
D-IIO/D-T FROM 25 OC		25.00	27.50	32.50	27.50	PA/OC
IIO AT 20,-20, 0		500.0M	1.000	1.750	1.500	NA
D-IIO/D-T FROM 25 OC		35.00	28.00	42.50	37.50	PA/OC
IIO AT 5, -5, 0		500.0M	175.0M	1.000	2.250	NA
D-IIO/D-T FROM 25 OC		35.00	11.75	25.75	45.00	PA/OC
IIB(+) AT 35, -5,-15		-2.750	-2.700	-2.750	-3.750	NA
IIB(+) AT 5,-35, 15		10.75	11.35	14.22	13.75	NA
IIB(+) AT 20,-20, 0		8.250	9.500	10.25	9.500	NA
IIB(+) AT 5, -5, 0		6.250	5.925	6.250	7.000	NA
IIB(-) AT 35, -5,-15		-5.000	-4.500	-5.250	-4.750	NA
IIB(-) AT 5,-35, 15		11.75	11.65	12.75	13.25	NA
IIB(-) AT 20,-20, 0		8.750	8.000	9.250	8.000	NA
IIB(-) AT 5, -5, 0		5.000	5.275	4.750	3.000	NA
PSRR(+)		-7.500	-6.850	500.0M	-4.000	UV/V
PSRR(-)		-15.50	-19.25	-10.00	-14.00	UV/V
CMR AT VCM = +-15V		104.4	99.22	101.2	103.5	DB
ICC AT VCC = +-20V		-1.680	-1.675	-1.675	-1.670	MA
ICC AT VCC = +-15V		-1.525	-1.520	-1.520	-1.515	MA
IOS(+)		-15.95	-16.10	-16.20	-16.05	MA
IOS(-)		8.220	8.410	8.125	7.990	MA
VOPP(+)	RL=10K	19.30	19.30	19.30	19.25	V
VOPP(-)	RL=10K	-18.15	-18.10	-18.10	-18.15	V
VOPP VLT SWING	RL=10K	37.45	37.40	37.40	37.40	V
VOPP(+)	RL=2K	17.75	17.75	17.75	17.75	V
VOPP(-)	RL=2K	-16.55	-16.60	-16.60	-16.60	V
VOPP VLT SWING	RL=2K	34.30	34.35	34.35	34.35	V
AVS(+)	RL=10K	-187.5	-272.7	-272.7	-200.0	V/MV
AVS(+)	RL=2K	-230.8	-250.0	-214.3	-250.0	V/MV
AVS(-)	RL=10K	-3.000K	-1.500K	-600.0	-750.0	V/MV
AVS(-)	RL=2K	4.021	4.115	3.559	3.341	V/MV
AVS AT +-5V	RL=10K	2.867	-27.21	2.395	2.837	V/MV
AVS AT +-5V	RL=2K	1.754	2.141	1.575	1.770	V/MV

Table 3-3. LM148 data sheet (Continued)

STATS AT 1 FROM 148ALL.LOG:OPA 16:15:00 11 APR 77
VIO AT 5,-35, 15 148; TEMP = -55 OC

LOWEST VALUE = 32.00000M HIGHEST VALUE = 2.340000
MEAN DEVIATION = 407.4358M MEAN = 689.3608M
STANDARD DEVIATION = 538.9003M NUMBER OF SAMPLES = 56

PERCENT IN ONE SIGMA = 75.00
PERCENT IN TWO SIGMA = 94.64
PERCENT IN THREE SIGMA = 98.21

NUMBER OF MEASUREMENTS BETWEEN

0.000	AND	120.0M	=	5
120.0M	AND	240.0M	=	6
240.0M	AND	360.0M	=	7
360.0M	AND	480.0M	=	6
480.0M	AND	600.0M	=	5
600.0M	AND	720.0M	=	5
720.0M	AND	840.0M	=	7
840.0M	AND	960.0M	=	4
960.0M	AND	1.080	=	2
1.080	AND	1.200	=	0
1.200	AND	1.320	=	1
1.320	AND	1.440	=	0
1.440	AND	1.560	=	2
1.560	AND	1.680	=	3
1.680	AND	1.800	=	0
1.800	AND	1.920	=	0
1.920	AND	2.040	=	1
2.040	AND	2.160	=	1
2.160	AND	2.280	=	0
2.280	AND	2.400	=	1

Table 3-4. Statistical summary of V_{IO} at V_{CM} = -15V and $T_A = -55^{o}C$

3.3.4 Data Analysis

Thirty-five summary sheets were generated on each device type for a single temperature. Next, the statistical summary sheets were reviewed and key information was transfered to two hand-written forms. For each parameter, common mode voltage and temperature condition the following values were recorded:

Data Value Low
Data Value High
Mean Value $\overline{X}$
Standard Deviation
% Population in $\overline{X} \pm 2\sigma$
% Population in $\overline{X} \pm 3\sigma$
Spec Limit Low
Spec Limit High

The failures were then sought out where the data exceeded the specified limits as recommended by the JC-41 Committee. A final data reduction step was to record and compare the data range values on another sheet with recommended JC-41 limits. Failures were identified on the sheets in two ways:

(1) If the failure was a single event, it was thrown out and bracket ( ) marks were put on the next lower in-spec value.

(2) If a number of failures occured on a parameter, the extreme failed limit was circled and in an adjacent note section the ratio of failed to tested devices was recorded (i.e., 5/56 means 5 out of 56 failed).

After both types of hand-written data summaries were completed, the failures were traced to the individual device data sheets as in table 3-3. All failures were identified with a yellow marker pen. At this stage of the device failures were plainly evident on the original data sheets. Relationships between failures could be observed and evaluated. Certain device deficiencies yielded more than one failure. For instance, one op amp failed V_{IO} at low common mode voltage, PSRR (+) and CMR. Since CMR and PSRR are calculated from changes in offset voltage conditions it is not surprising to have related failures among these parameters for some parts. A breakdown of one of the front-end transistor base-collector junctions is the deficiency most likely to cause these three test failures.

Vendor Type	No. Tested	No. Failed
LM148	14	7
4741	17	3
4156	7	3
4136	18	8

3.3.5 Bench Tests

Transient response, slew rate, channel separation and noise were parameters that had to be tested on the bench. Summaries of the data are tabulated in 3.4 of this report. All of the parts were within the specified limits with the exception of 4136 transient response overshoot. The reason for the 4136 failures is that extra parasitics were introduced by an additional socket card used to convert the 4136 pin out to the standard pin out of the other devices.

3.4 Tabulation of Electrical Characteristics

3.4.1 MIL-M-38510/110 Electrical Performance Characteristics Table (Table I in the specification).

This specification table shows the parameters, conditions and limits for the quad op amp devices in MIL-M-38510/110 table I. Table 3-5, consisting of two pages and notes, shows this information in this report.

3.4.2 Quad Op Amp Data Sheets

The reduced characterization data was transferred to a number of tables according to device type, temperature and type of testing. This data is indexed in table 3-7.

The static tests were all done automatically on RADC's S-3260 IC tester. Shown on the static test sheets are the extreme data values and statistical parameters of the data population. Spec limits and failures are also shown. Three types of forms are used to display the summarized data. They are as follows:

(1) Device type __ data versus recommended limits.
(2) Device type __ static test data at __°C.
(3) Device type __ dynamic test data.

Form (1) contrasts the limits of Form (2) data against the recommended limits. Channel separation and noise are not dynamic tests, but they are shown here because they were not taken with the S-3260 automatic tester.

3.5 Oscillographs of Electrical Characterization

A number of oscillographs were taken of device characteristics as observed on a Tektronix Type 577 curve tracer. These oscillographs show typical parameter to parameter relationships that are not as readily seen with tabulated discrete data. Linearity of the lack of it is apparent in these curves. A directory of typical curves is shown in table 3-28.

Table 3-5. Electrical performance characteristics

Characteristics	Symbol	Conditions (Paragraph 3.4 and Figure 3-5 Unless Otherwise Specified)
Input Offset Voltage	V_{IO}	1/ $T_A = 25^{\circ}C$ / $-55^{\circ}C \leq T_A \leq 125^{\circ}C$
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\triangle T_A$ from $-55^{\circ}C$ to $+25^{\circ}C$ / $\triangle T_A$ from $+25^{\circ}C$ to $125^{\circ}C$
Input Offset Current	I_{IO}	R_S = 20 KΩ 1/ $25^{\circ}C \leq T_A \leq 125^{\circ}C$ / $T_A = -55^{\circ}C$
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	$\triangle T_A$ from $-55^{\circ}C$ to $+25^{\circ}C$ / $\triangle T_A$ from $+25^{\circ}C$ to $+125^{\circ}C$
Input Bias Current	$+I_{IB}$	R_S = 20 KΩ 1/ $25^{\circ}C \leq T_A \leq 125^{\circ}C$ / $T_A = -55^{\circ}C$
	$-I_{IB}$	R_S = 20 KΩ 1/ $25^{\circ}C \leq T_A \leq 125^{\circ}C$ / $T_A = -55^{\circ}C$
Power Supply Rejection Ratio	+PSRR	$+V_{CC}$ = 10V, $-V_{CC}$ = 20V for -01 thru 04, $+V_{CC}$ = 20V for -05
	-PSRR	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V for -01 thru 04
Input Voltage Common Mode Rejection	CMR	Common Mode Range = 30V 4/
Output Short Circuit Current (for Positive Output)	$I_{OS(+)}$	2/ $+V_{CC}$ = +15V for -01 thru 04 / $+V_{CC}$ = 30V for -05 / $t \leq 25$ ms
Output Short Circuit Current (for Negative Output)	$I_{OS(-)}$	(1 amplifier only shorted to ground)
Supply Current	I_{CC}	$\pm V_{CC}$ = $\pm$15V for -01 thru 04 3/ $T_A = -55^{\circ}C$ / $T_A = 25^{\circ}C$ / $T_A = 125^{\circ}C$ / $+V_{CC}$ = +30V for -05

Table 3-5. Electrical performance characteristics

Limits								
-01, 02		-03		-04		-05		
Min	Max	Min	Max	Min	Max	Min	Max	Units
-5 -6	5 6	-3 -5	3 5	-5 -6	5 6	-5 -7	5 7	mV
-25 -25	25 25	-20 -20	20 20	-25 -25	25 25	-30 -30	30 30	uV/°C
-25 -75	25 75	-30 -75	30 75	-75 -150	75 150	-30 -90	30 90	nA
-500 -200	500 200	-500 -200	500 200	-1000 -500	1000 500	-700 -600	700 600	PA/°C
1 1	100 325	-200 -325	-1 -1	-250 -400	-1 -1	-150 -300	-1 -1	nA
1 1	100 325	-200 -325	-1 -1	-250 -400	-1 -1	-150 -300	-1 -1	nA
-100	100	-100	100	-100	100	-100	100	uV/V
-100	100	-100	100	-100	100	-	-	uV/V
76	-	76	-	76	-	76	-	dB
-55	-	-80	-	-80	-	-70	0	mA
-	55	-	80	-	80	-	-	mA
- - -	4.5 3.6 3.6	- - -	13 11 11	- - -	13 11 11	- - -	4 3 3	mA mA mA

Table 3-5. Electrical performance characteristics (Continued)

Characteristics	Symbol	Conditions (Paragraph 3.4 and Figure 3-5 Unless Otherwise Specified)	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC}$ = +20V (01-04) V_{CC} = 30V (05)	R_L = 10 KΩ R_L = 2 KΩ
Open Loop Voltage Gain (Single Ended)	$A_{VS}(+)$ $A_{VS}(-)$	V_O = +15V @ R_L = 10K, 2K (01-04) V_O = 1 to 26V @ R_L = 10K (05) V_O = 1 to 16V @ R_L = 2K (05)	T_A = 25°C -55°C ≤ T_A ≤ 125°C
	A_{VS}	$\pm V_{CC}$ = +5V, V_O = ±2V (-01 thru 04) V_{CC} = 5V, V_O = 1V to 3V (-05) R_L = 2 KΩ, 10 KΩ	T_A = 25°C -55°C ≤ T_A ≤ 125°C
Output Voltage Low	V_{OL}	V_{CC} = 30V	R_L = 10 KΩ
Output Voltage High	V_{OH}		I_{OH} = 10 mA
Output Voltage Low	V_{OL}		I_{OL} = 5 mA
Output Voltage High	V_{OH}	V_{CC} = 4.5V	I_{OH} = 10 mA
Output Voltage Low	V_{OL}		I_{OL} = 8 uA
Transient Response (Risetime)	$TR(t_r)$	$\pm V_{CC}$ = ±20V (-01 thru 04) V_{CC} = 30V (-05)	A_V = 1, V_{IN} = 50 mV A_V = 5, V_{IN} = 50 mV
(Overshoot)	$TR(OS)$	C_F = 10 pF	Overshoot
Slew Rate	$SR(+)$ $SR(-)$	A_V = 1 (-01, 03, 04, 05) A_V = 5 (-02)	A_V = 1 A_V = 5 A_V = 1 A_V = 5
Noise (Breadband)	$N_1(BB)$	T_A = 25°C	R_S = 50Ω
Noise (Popcorn)	$N_1(PC)$		R_S = 20 KΩ
Channel Separation	CS	T_A = 25°C	

Table 3-5. Electrical performance characteristics (Continued)

Limits								
-01, 02		-03		-04		-05		
Min	Max	Min	Max	Min	Max	Min	Max	Units
+16 ±15	- -	+16 ±15	- -	+16 ±15	- -	+27 ±26	- -	V
50 25	- -	50 25	- -	50 25	- -	50 25	- -	V/mV
10 10	- -	10 10	- -	10 10	- -	10 5	- -	
-	-	-	-	-	-	-	20	mV
- -	- -	- -	- -	- -	- -	25 -	- 3	V
- -	- -	- -	- -	- -	- -	2.4 -	- 0.4	
- -	1.0 1.0	- -	0.2 -	- -	0.3 -	- -	1.0 -	uS
-	25	-	25	-	25	-	40	%
0.2 0.8 0.2 0.8	- - - -	0.8 - 0.8 -	- - - -	0.6 - 0.6 -	- - - -	0.1 - 0.1 -	- - - -	V/uS
-	15	-	5	-	5	-	15	uVrms
-	40	-	50	-	50	-	50	uVpk
80	-	80	-	80	-	80	-	dB

Table 3-5. Electrical performance characteristics (Continued)

NOTES:

1/ For -01 thru -04 limits shall be tested at V_{CM} = 0, +15V and -15V for $+V_{CC}$ = +20V, at V_{CM} = 0V for V_{CC} = 5V. For -05 limits shall be tested at V_{CM} = 0 and 28V for V_{CC} = 30V and at V_{CM} = 0V for V_{CC} = 5V.

2/ Continuous limits will be considerably lower and apply for $-55^{\circ}C \leq T_A \leq 75^{\circ}C$.

3/ I_{CC} limits are the total for all four amplifiers at no loads connected as grounded followers.

4/ CMR is determined by measuring input offset voltage under the following conditions for the devices:

Offset Voltage Condition	Device 01, 02, 03 04			Device 05			Units
	$+V_{CC}$	$-V_{CC}$	V_O	$+V_{CC}$	$-V_{CC}$	V_O	
1	35	-5	15	30	0	-15	V
2	5	-35	-15	2	28	15	V

3.6 Discussion

3.6.1 General Comments

The quad op amp specification is similar to MIL-M-38510/101 on single operational amplifiers. The same parameters apply to both kinds of devices. Only the type 05 (LM124) required the developing of several new tests. The type 05 can be operated from a single 5V power supply, and with a pull-down resistor can be used to interface with TTL logic. In general, the quad op amps are not so good as their single counterparts except for supply current drain and circuit density. Because there are four circuits in a package instead of one, somewhat lower tolerances are justified than for single op amps.

The characterization program did not result in many surprises. Even though much data was taken and examined, hardly any changes were made to the JC-41 Committee's recommended limits. There are at least two reasons for this result :

(1) If the data on 50 or so op amps indicates a range well below the JC-41 recommended limits, the limited data quantity is not sufficient to tighten the specification. It does, however, warrant discussion and reconsideration by the JC-41 Committee.

(2) If the data shows that the range is close to the specification limits, one is reluctant to degrade this specification, especially if it is useful to the user.

In general the data shows the parameters to be in agreement with the specification limits. Exceptions, if any, will be pointed out later on. Obviously, one failure in a device is enough to reject that device from acceptance. In a worst case situation, those failures would be scattered to cause the maximum number of devices to be rejected. The data tends to show a clustering effect where the failures are together in a few devices. Thus the first failure causes the device to be rejected and the remaining failures in that device are "free" with respect to yield.

3.6.2 Parameter Failures

Table 3-6 shows a summary of all the parameter failures for the devices tested. Comments relative to those failures are as follows:

3.6.2.1

V_{IO} - With the exception of the 4156, all of the devices had a few V_{IO} failures. These were associated with PSRR and CMR failures in some cases such as the input transistor base-collector junction breakdown.

Table 3-6. Summary of static test failures

Parameter Symbol	LM148			4741			4156			4136		
	Temp			Temp			Temp			Temp		
	-55	25	125	-55	25	125	-55	25	125	-55	25	125
V_{IO}	1/56	1/56	1/56	5/80	X	X	X	X	X	1/80	X	4/72
$\Delta V_{IO}/\Delta T$	X	-	X	7/80	-	X	X	X	X	-	-	-
I_{IO}	X	X	X	X	X	X	X	X	X	3/80	2/72	2/72
$\Delta I_{IO}/\Delta T$	X	-	X	X	-	X	X	X	X	-	-	-
$+I_{IB}$	13/56	12/56	13/56	X	1/80	X	X	X	X	6/80	2/72	6/72
$-I_{IB}$	12/56	≈8/56	12/56	X	1/80	X	X	X	X	3/80	1/72	3/72
+PSRR	10/56	1/56	9/56	4/80	X	X	X	X	X	X	X	X
-PSRR	X	X	8/56	4/80	X	X	X	X	X	X	X	X
CMR	1/56	1/56	1/56	3/80	X	X	X	X	X	1/80	X	X
$I_{OS(+)}$	X	X	X	X	X	X	X	X	X	18/80	6/72	X
$I_{OS(-)}$	X	X	X	X	X	X	X	X	X	19/80	X	X
I_{CC}	X	X	X	X	X	X	X	X	X	X	X	X
$V_{OP(+)}$	X	X	X	4/80	X	X	X	X	X	X	X	X
$V_{OP(-)}$	X	X	X	4/80	X	X	X	X	X	X	X	X
$A_{VS(+)}$	X	X	X	X	X	X	X	X	X	X	X	X

X = NO FAILURES

Table 3-6. Summary of static test failures (Continued)

Parameter Symbol	LM148			4741			4156			4136		
	Temp			Temp			Temp			Temp		
	-55	25	125	-55	25	125	-55	25	125	-55	25	125
$\Delta VS(-)$	X	X	X	X	X	7/80	X	X	16/40	X	X	X
ΔVS	56/56	56/56	56/56	80/80	X	X	40/40	39/40	11/40	80/80	78/80	X
Total Failures (Excluding AVS)	7/14			3/17			0/10			8/18		

X = NO FAILURES

3.6.2.2

$\Delta V_{IO}/\Delta T$ - Only the 4741 had these failures. Three devices which had these failures in one or more op amps also had V_{IO} failures.

3.6.2.3

I_{IO} - The 4136 devices had a few I_{IO} failures, which also contained I_{IB} failures.

3.6.2.4

$\Delta I_{IO}/\Delta T$ - A 4136 device had this failure along with I_{IO} and I_{IB} failures.

3.6.2.5

$+I_{IB}$, $-I_{IB}$ - Wrong polarity bias current was the worst parameter for the LM148. It occurred in three of 14 devices. In the affected devices, most of the 12 op-amp/temperature combinations exhibited the failure. PSRR failures also occurred in these same devices. During a curve tracer analysis of a device with the problem, the device destroyed itself when the negative common mode range limit was approached. An autopsy of the device showed a burned-open circuit between pin 4 (+VCC terminal) and the emitter of the diode-connected transistor, which sources current to LM148 front end. Figure 3-6 shows a photomicrograph of the damaged IC area.

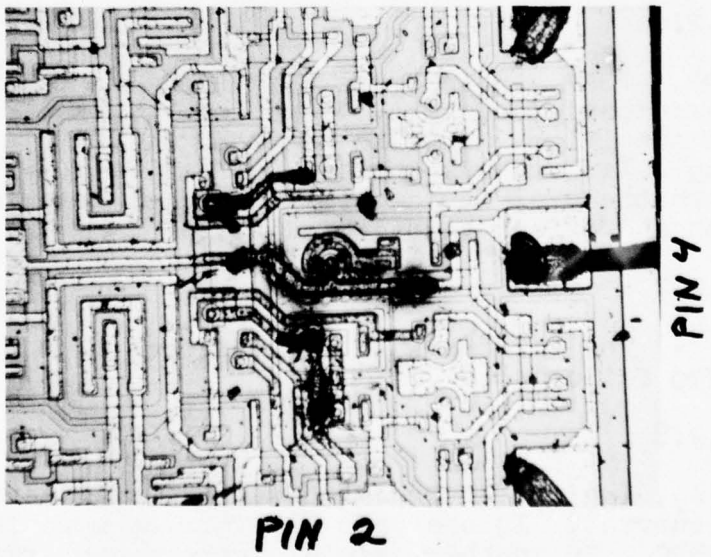


Figure 3-6 . LM148 with burned-open VCC conductor following reverse bias current breakdown.

3.6.2.5 (Continued)

Another device with wrong polarity bias current was examined more carefully against a normal device. A comparison display of bias current versus common mode voltage is shown in figure 3-7.

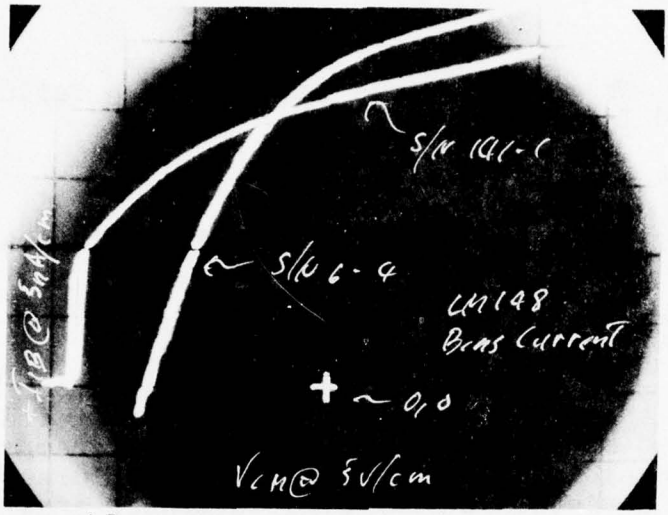


Figure 3-7. LM148 bias current versus common mode voltage in good and bad devices.

The oscillograph shows that the bias current of S/N 6-4 (op amp 4 in S/N 6) changes polarity at -13V of input common mode voltage. With a good device, on the other hand, the bias current remains positive beyond the -15V common mode range limit, and then never falls below 0V.

3.6.2.6

+PSRR, -PSRR - Failures with positive power supply rejection accompanied offset voltage and common mode rejection failures in the LM148. It also happened at -55°C with an LM148 having wrong polarity bias current. -PSRR failures are less common. With the 4741 devices PSRR failures were tandem with bias current and offset voltage failures.

3.6.2.7

CMR - The LM148's with CMR failures also had related +PSRR and V_{IO} failures.

3.6.2.8

$I_{OS}(+)$, $I_{OS}(-)$ - The 4136 was the only device seen with excess I_{OS} current. In one case all four op amps failed at -55°C and 25°C. In another case a single op amp failure occurred at 25°C. I_{OS} failures seem to be independent of any other parameter failures.

3.6.2.9

I_{CC} - No I_{CC} failures on any devices were observed. In trying to correlate S-3260 readings with 577 curve tracer readings, a 2:1 discrepancy was observed. This was resolved when it was determined that the S-3260 method tested the devices as grounded emitter followers versus undriven devices in the curve tracer.

3.6.2.10

$V_{OP}(+)$, $V_{OP}(-)$ - Only the 4741 exhibited a few V_{OP} failures. These failures were in $V_{OP}(-)$ and were sign rather than magnitude related. Many other parameters were also bad with these device at -55°C only.

3.6.2.11

$A_{VS}(+)$, $A_{VS}(-)$ - A few $A_{VS}(-)$ failures occurred in the 4741 at 125°C. These were isolated failures. Similar border line failureswere seen in two of seven 4156's. Thermal effects mask these parameters, especially when a 2K Ω load is used.

3.6.2.12

A_{VS} - A_{VS} checks the open loop gain with $\pm$5V supplies. This was the most prevalent failure of all. A few of these failures were spot checked on the 577 curve tracer without the failures being confirmed. A problem with the S-3260 is suspected.

3.6.2.13

$TR(t_r)$, TR(OS) - Transient response rise time and overshoot were measured normally. The data except for 4136 overshoot was well within the spec limits. As mentioned earlier, an extra conversion socket was used to make the 4136 pin-out the same as that of the other devices. The parasitics associated with the cross-wiring are believed responsible for the failures.

3.6.2.14

SR(+), SR(-) - Slew rate for both directions on all devices was satisfactory. A 20% margin exists between the limit specification and the low data point of the 4156. The other devices have even wider margins.

3.6.2.15

CS - All devices passed DC channel separation with at least 23 dB of margin. This test looks for thermal coupling between the four op amps of the device.

3.6.2.16

$N_1(BB)$, $N_1(PC)$ - Both broadband and popcorn noise were measured with the 577 curve tracer on a number of devices. No failures were observed.

3.6.3 Tektronix S-3260 Histograms

Figures 3-8 and 3-9 show histograms of V_{IO} offset voltage for two different conditions of supply voltage, common mode voltage and temperature. Similar histograms were generated for most of the other parameter data. In contrast to tabulated information such as in table 3-4, histograms give a much better picture of the data distribution with respect to the specified limits.

3.7 Conclusions

The results of the quad operational amplifier characterization effort show that the data, in general, supports the recommended specification limits proposed by JEDEC JC-41. Since the quad op amps have a close resemblance to single op amps, the parameters necessary to characterize the devices are the same. Channel separation is a necessary additional parameter. Device type 05 (LM124) has a few new parameters to specify the output source and sink drive capabilities of the device for TTL and related loads.

The new MIL-M-38510/110 quad op amp specification is technically complete and accurate. Vendors who are represented by the JC-41 Committee have had a rough draft copy of this spec for a month as of the writing of this report.

3.8 Recommendations for Future Effort

The characterization effort on the quad op amps has shown the value and need for automatic test methods to accumulate device data. Relatively little time is required to take the raw data and reduce it once the proper hardware and software has been developed.

A big improvement is desirable in formating and contrasting the data so that failures and anomalies stand out.

Since the location of device failures in the data is an important objective, one software improvement would be to have the computer print out an asterisk (*) adjacent to every failure in the device data sheet (i.e., table 3-3). These failures would be based on a comparison with the specified limits. Another improvement would be histograms at all three temperatures on the same sheet.

Open-loop gain as observed in this program appears to be a maverick parameter. A credibility gap exists between the 25V/mV minimum spec limit and real data where values from 15000V/mV to -3750 V/mV are typical on a single device at one temperature. The screening value of this test method is questionable. On the other hand. vendors advocate the present open-loop AVS test method as opposed to a closed-loop gain test. Since thermal effects are very dominant in open-loop gain tests, a recommended compromise is to do these tests at very light loads (i.e., 50 KΩ and 10.KΩ instead of 10KΩ and 2 KΩ).

Bi-FET op amps is another species of similar linear devices which should be considered for characterization and possible future slash sheet action.

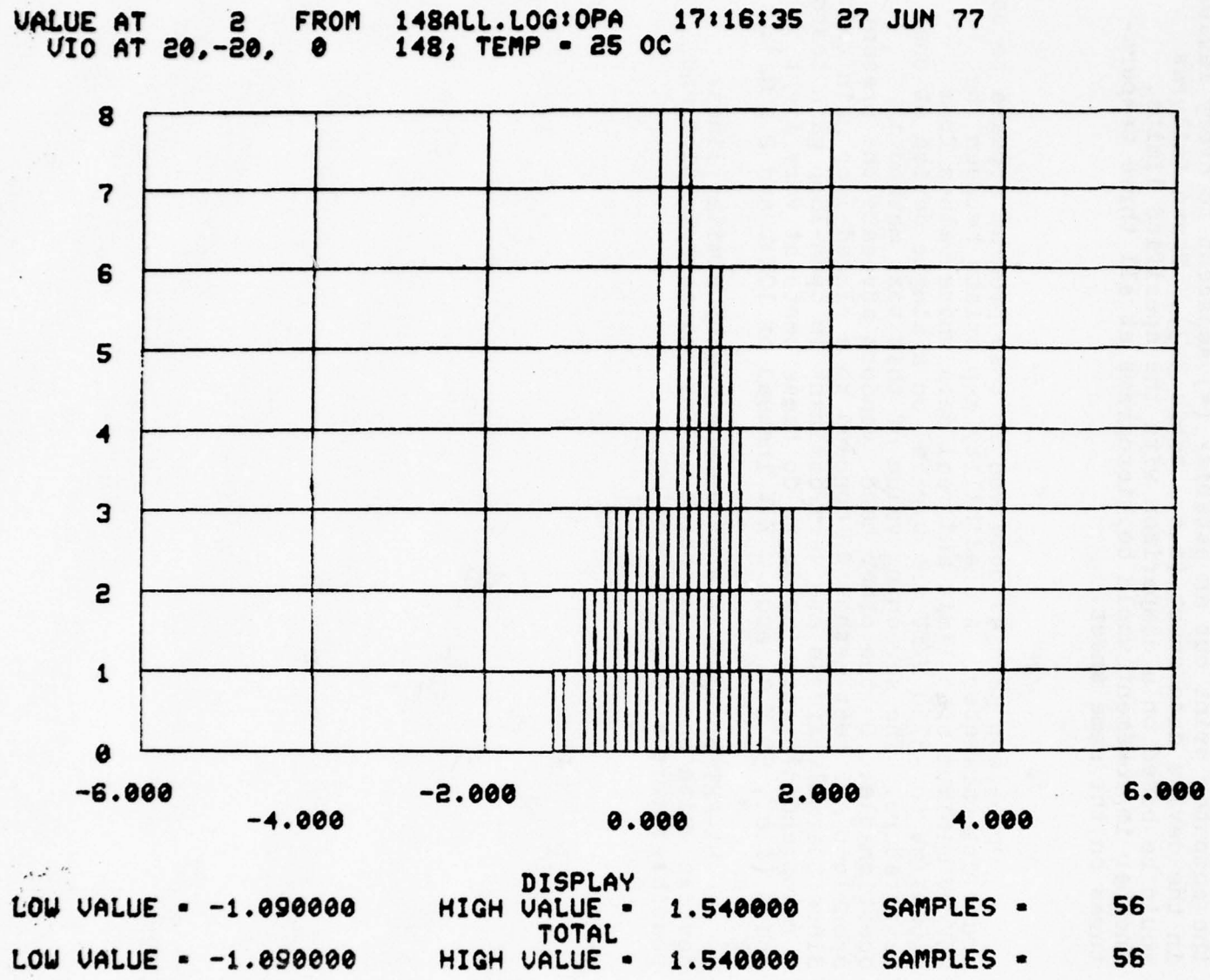


Figure 3-8. LM148 V_{IO}, 0V common mode, 25°C histogram

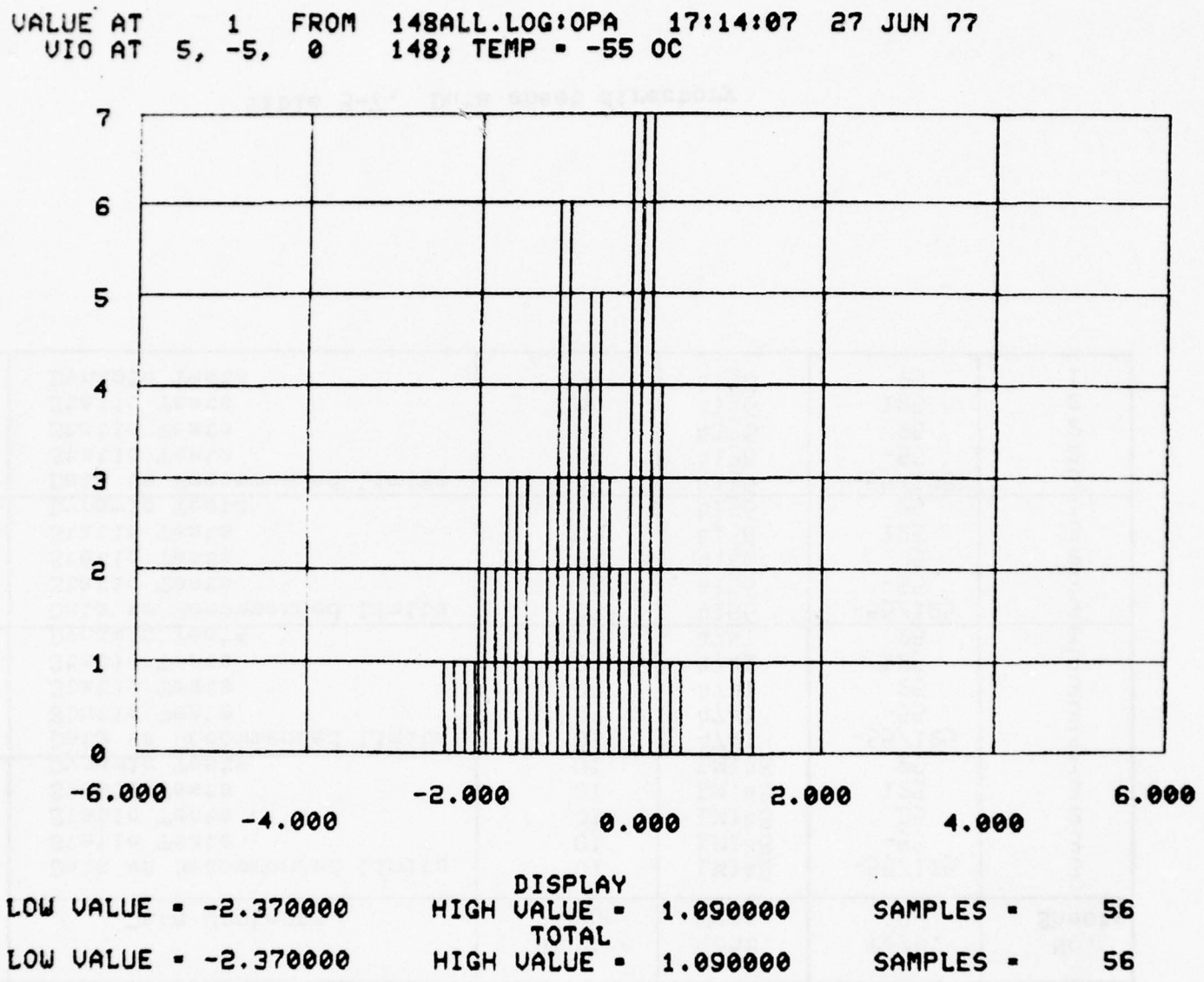


Figure 3-9. LM148 V_{IO}, Low V_{CC}, -55°C histogram

Table No.	Data Contents	Device Type	Comm. Type	Temp. °C	No. Sheets
3-8	Data vs Recommended Limits	01	LM148	-55/125	3
3-9	Static Tests	01	LM148	-55	3
3-10	Static Tests	01	LM148	25	2
3-11	Static Tests	01	LM148	125	3
3-12	Dynamic Tests	01	LM148	25	1
3-13	Data vs Recommended Limits	03	4741	-55/125	3
3-14	Static Tests	03	4741	-55	3
3-15	Static Tests	03	4741	25	3
3-16	Static Tests	03	4741	125	3
3-17	Dynamic Tests	03	4741	25	1
3-18	Data vs Recommended Limits	03	4156	-55/125	3
3-19	Static Tests	03	4156	-55	3
3-20	Static Tests	03	4156	25	2
3-21	Static Tests	03	4156	125	3
3-22	Dynamic Tests	03	4156	25	1
3-23	Data vs Recommended Limits	04	4136	-55/125	3
3-24	Static Tests	04	4136	-55	2
3-25	Static Tests	04	4136	25	2
3-26	Static Tests	04	4136	125	2
3-27	Dynamic Tests	04	4136	25	1

Table 3-7. Data sheet directory

Table 3-8. Device type 01 (LM148) data versus recommended limits

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
V_{IO}	$V_{CM} = +15V, -15V,$ 0V @ $V_{CC} = \pm 20V$ $V_{CM} = 0V$ @ $V_{CC} = \pm 5V$	-55	-6	6	-2.37	(3.1)	-6	6	mV
		25	-5	5	-1.46	(2.0)	-5	5	
		125	-6	6	-.97	2.67	-6	6	
$\frac{\Delta V_{IO}}{\Delta T}$	$V_{CM} = 0$	-55/25	-25	25	-15.6	7.55	-25	25	uV/°C
		25/125	-25	25	-2.69	11.2	-25	25	
I_{IO}	(Same as for V_{IO})	-55	-75	75	-12.8	19.8	-75	75	nA
		25	-25	25	-10	10.5	-25	25	
		125	-75	75	-5	9.15	-25	25	
$\frac{\Delta I_{IO}}{\Delta T}$	$V_{CM} = 0$	-55/25	-500	500	-196	107	-400	400	PA/°C
		25/125	-200	200	-12.7	72.5	-200	200	
$+I_{IB}$	(Same as for V_{IO})	-55	1	325	-15	96	1	325	nA
		25	1	100	-5.35	76.5	1	100	
		125	1	325	-5.15	49	1	100	
$-I_{IB}$	(Same as for V_{IO})	-55	1	325	-11	92.8	1	325	nA
		25	1	100	-2.25	65.6	1	100	
		125	1	325	-7.25	39.5	1	100	
+PSRR		-55	-100	100	11.1	(166)	-100	100	uV/V
		25	-100	100	2	(57)	-100	100	
		125	-100	100	-19.2	133	-100	100	
-PSRR		-55	-100	100	5	161	-100	100	uV/V
		25	-100	100	-7	48.2	-100	100	
		125	-100	100	-27.8	-3.75	-100	100	

Table 3-8. Device type 01 (LM148) data versus recommended limits (Continued)

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
CMR		-55	76	-	88.5	156	76	-	dB
		25	76	-	(98.9)	160	76	-	
		125	76	-	(95.35)	129.5	76	-	
$I_{OS(+)}$	$V_{CC} = \pm 15V$	-55	-55	-	-35.3	-18.9	-55	-	mA
		25	-55	-	-31	-23.3	-55	-	
		125	-55	-	-19.45	-13.6	-55	-	
$I_{OS(-)}$	$V_{CC} = \pm 15V$	-55	-	55	23.6	34.5	-	55	mA
		25	-	55	15.6	22.7	-	55	
		125	-	55	6.52	9.60	-	55	
I_{CC}	$V_{CC} = \pm 20V$	-55	-	6	3.26	4.25	-	6	mA
		25	-	4.5	2.4	3.18	-	4.5	
		125	-	4.5	1.65	2.17	-	4.5	
I_{CC}	$V_{CC} = \pm 15V$	-55	-	4.5	2.99	3.88	-	4.5	mA
		25	-	3.6	2.21	2.89	-	3.6	
		125	-	3.6	1.50	1.96	-	3.6	
$V_{OP(+)}$	$R_L = 10\ K\Omega$	-55	16	-	19	19.05	16	-	V
		25	16	-	-	-	16	-	
		125	16	-	19.25	19.30	16	-	
$V_{OP(-)}$	$R_L = 10\ K\Omega$	-55	-	-16	-17.1	-16.9	-	-16	V
		25	-	-16	-17.6	-17.4	-	-16	
		125	-	-16	-18.2	-17.95	-	-16	
$V_{OP(+)}$	$R_L = 2\ K\Omega$	-55	15	-	17.75	18.2	15	-	V
		25	15	-	17.75	17.95	15	-	
		125	15	-	17.75	17.85	15	-	

Table 3-8. Device type 01 (LM148) data versus recommended limits (Continued)

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
$V_{OP(-)}$	R_L = 2 K	-55	-	-15	-16.6	-16.25	-	-15	V
		25	-	-15	-16.85	-16.40	-	-15	
		125	-	-15	-16.9	-14.2	-	-15	
$A_{VS(+)}$	R_L = 10 K	-55	25	-	-435	30K	25	-	V/mV
		25	50	-	-3.75K	30K	50	-	
		125	25	-	-10K	9K	25	-	
$A_{VS(-)}$	R_L = 10 K	-55	25	-	-3.7K	15K	25	-	V/mV
		25	50	-	-30K	30K	50	-	
		125	25	-	-30K	9K	25	-	
$A_{VS(+)}$	R_L = 2 K	-55	25	-	-882	3K	25	-	V/mV
		25	50	-	-465	9K	50	-	
		125	25	-	-3.3K	9K	25	-	
$A_{VS(-)}$	R_L = 2 K	-55	25	-	-5K	10K	25	-	V/mV
		25	50	-	-10K	5K	50	-	
		125	25	-	1.29	10	25	-	
A_{VS}	$V_{CC} = +5V$, R_L = 10 K	-55	10	-	.562	.738	10	-	V/mV
		25	10	-	840	1.976	10	-	
		125	10	-	-19.7	111	10	-	
A_{VS}	$V_{CC} = \pm 5V$, R_L = 2 K	-55	10	-	.536	.672	10	-	V/mV
		25	10	-	.761	1.38	10	-	
		125	10	-	-26.3	20.9	10	-	

NOTES: 1/ Failed limits are circled.
2/ Bracketed data excludes failed data. For instance one sample out of 56 was rejected.

Table 3-9. Device type 01 (LM148) static test data at -55°C

Parameter Symbol	Voltages ±V_{CC}	Voltages V_{CM}	Data (Sample Size = 56) Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Spec. Limits Min	Max	Units	Notes
V_{IO}	20	15	-1.00	(3.1)	.875	2.0	98.21	98.21	-6	6	mV	1/ 14.3
	20	-15	-1.02	2.34	.454	.75	96.43	100				
	20	0	-1.00	2.54	.551	.805	96.43	100				
	5	0	-2.37	1.09	-.741	.727	94.6	100				
I_{IO}	20	15	-12.75	16.02	-4.01	4.34	94.6	98.2	-75	75	nA	
	20	-15	-11.25	19.83	-4.09	4.89	96.4	98.2				
	20	0	-10.8	17.3	-4.21	4.54	96.4	98.2				
	5	0	-9.73	13.25	-3.15	3.81	96.4	98.2				
$+I_{IB}$	20	15	-15	73.47	25.01	23.80	98.21	100	1	325	nA	2/ I3/56
	20	-15	31.75	95.98	55.53	14.8	96.43	100				
	20	0	24	85.67	48.08	14.59	96.43	100				
	5	0	16.2	59.37	32.37	9.38	96.43	100				
$-I_{IB}$	20	15	-11	68.25	28.79	23.27	100	100	1	325	nA	2/ I2/56
	20	-15	37.75	99.75	59.7	13.89	96.43	100				
	20	0	30.75	84.0	52.23	13.52	96.43	100				
	5	0	21.87	60	35.08	8.32	96.43	100				
+PSRR	20		11.1	247.1	54.55	48.23	94.64	98.21	-100	100	uV/V	2/10/56
-PSRR	20		5.0	160.9	48.37	39.85	92.86	100	-100	100	uV/V	
CMR	20	±15	(83.5)	155.56	108.68	12.68	96.43	96.43	76	-	dB	1/66.2
$I_{OS(+)}$	15	0	-35.25	-18.9	-26.87	4.43	100	100	-55	-	mA	
$I_{OS(-)}$	15	0	23.6	34.5	28.96	3.43	100	100	-	55	mA	
I_{CC}	20	0	-4.25	-2.26	-3.81	.302	100	100	-	6	mA	
	15	0	-3.88	-2.99	-3.48	.272	100	100	-	4.5		

Table 3-9. Device type 01 (LM148) static test data at -55°C (Continued)

Parameter Symbol	Voltages $\pm V_{CC}$	Voltages R_L	Data (Sample Size = 56) Low	High	$\bar{X}$	σ	$\%(\pm 2\sigma)$	$\%(\pm 3\sigma)$	Spec. Limits Min	Spec. Limits Max	Units	Notes
$V_{OP}(+)$	20	10K	19.0	19.05	19.02	.252	100	100	+16	-	V	
$V_{OP}(-)$	20	10K	-17.1	-16.9	-17.03	.381	98.21	98.21	-	-16	V	
$V_{OP}(+)$	20	2K	17.75	18.20	17.78	.117	92.86	92.86	+15	-	V	
$V_{OP}(-)$	20	2K	-16.6	-16.25	-16.46	.105	96.43	100	-	-15	V	
$A_{VS}(+)$	20	10K	-434.8	30.00K	1.268K	4.32K	96.43	96.43	25	-	V/mV	
$A_{VS}(-)$	20	10K	-3.75K	14.99K	908.29	3.077	92.86	98.21	25	-	V/mV	
$A_{VS}(+)$	20	2K	-88235	3.00K	324.25	635.26	96.43	96.43	25	-	V/mV	
$A_{VS}(-)$	20	2K	-4.99K	10.0K	-160.7	2.355K	92.86	96.43	25	-	V/mV	
A_{VS}	5	10K	.562	.738	.604	.034	94.64	96.43	25	-	V/mV	3/
A_{VS}	5	2K	.536	.672	.576	.030	92.86	98.21	10	-	V/mV	3/
A_{VS}											V/mV	
A_{VS}											V/mV	
$\frac{\Delta V_{IO}}{\Delta T}$	20		-15.6	7.55	-2.82	5.79	94.64	100	-25	25	uV/°C	
$\frac{\Delta I_{IO}}{\Delta T}$	20		-196.3	107.5	22.84	43.99	96.43	98.21	-500	500	PA/°C	

Table 3-9. Device type 01 (LM148) static test data at -55°C (Continued)

NOTES:

1/ One op amp failed this parameter. The failed limit is shown after the note and the next inside limit is bracketed in the data.

2/ More than one op amp failed this parameter. The number of failures is shown next.

3/ No op amp meets the spec.

Table 3-10. Device type 01 (LM148) static test data at 25°C

Parameter Symbol	Voltages		Data (Sample Size = 56)						Spec. Limits		Units	Notes
	±VCC	VCM	Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Min	Max		
V_{IO}	20	15	-1.085	(2.0)	.619	1.88	98.21	98.21	-5	5	mV	1/
	20	-15	-1.125	1.49	.253	.576	96.43	100				3.75
	20	0	-1.09	1.54	.325	.595	96.43	100				
	5	0	-1.465	.925	-.108	.578	98.21	100				
I_{IO}	20	15	-9.99	7.67	-2.684	2.434	94.64	96.43	-25	25	nA	
	20	-15	-7.075	10.48	-2.337	2.576	96.43	98.21				
	20	0	-6.70	9.099	-2.384	2.365	96.43	98.21				
	5	0	-5.35	7.050	-2.392	1.892	96.43	98.21				
$+I_{IB}$	20	15	-5.35	58.58	17.73	14.37	98.21	100	1	100	nA	2/
	20	-15	18.68	76.50	35.15	10.64	98.21	98.21				2/56
	20	0	13.63	69.08	30.49	10.19	98.21	98.21				
	5	0	10.08	46.50	19.36	6.37	98.21	98.21				
$-I_{IB}$	20	15	-2.25	49.75	20.52	13.93	98.21	100	1	100	nA	2/
	20	-15	20.75	65.58	37.66	9.87	96.43	100				8/56
	20	0	16.75	59.25	32.85	9.565	96.43	100				
	5	0	11.10	39.78	21.67	5.689	94.64	98.21				
+PSRR	20		1.999	(57)	19.06	26.14	98.21	98.21	-100	100	uV/V	1/189.8
-PSRR	20		-6.999	48.70	12.28	12.26	92.86	100	-100	100	uV/V	
CMR	20	±15	(98.9)	160.0	109.3	10.53	96.43	96.43	76	0	dB	1/66.49
$I_{OS(+)}$	15	0	-31.05	-23.35	-26.88	2.095	100	100	-55	-	mA	
$I_{OS(-)}$	15	0	15.60	22.75	18.85	2.220	100	100	-	55	mA	
I_{CC}	20	0	-3.18	-2.410	-2.838	.230	100	100	-	4.5	mA	
	15	0	-2.885	-2.205	-2.580	.206	100	100	-	3.6		

Table 3-10. Device type 01 (LM148) static test data at 25°C (Continued)

Parameter Symbol	Voltages		Data (Sample Size = 56)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	R_L	Low	High	$\bar{X}$	σ	$\%(\pm 2\sigma)$	$\%(\pm 3\sigma)$	Min	Max		
$V_{OP}(+)$	20	10K							+16	-	V	
$V_{OP}(-)$	20	10K	-17.60	-17.40	-17.51	.046	96.43	100	-	-16	V	
$V_{OP}(+)$	20	2K	17.75	17.95	17.76	.052	92.86	92.86	+15	-	V	
$V_{OP}(-)$	20	2K	-16.85	-16.40	-16.69	.137	96.43	100	-	-15	V	
$A_{VS}(+)$	20	10K	-3.75K	30.00K	1.463K	4.368K	98.21	98.21	50	-	V/mV	
$A_{VS}(-)$	20	10K	-3000K	30.00K	1.134K	6.404K	96.43	96.43	50	-	V/mV	
$A_{VS}(+)$	20	2K	-465.1	9.000K	740.0	1.36K	98.21	98.21	50	-	V/mV	
$A_{VS}(-)$	20	2K	-10K	5K	-670	1.93K	96.43	98.21	50	-	V/mV	
A_{VS}	5	10K	.840	1.976	1.034	.185	96.43	96.43	10	-	V/mV	3/
A_{VS}	5	2K	.761	1.38	.892	.102	96.43	96.43	10	-	V/mV	3/
A_{VS}											V/mV	
A_{VS}											V/mV	

NOTES:

1/ One op amp failed this parameter. The failed limit is shown after the note and the next inside limit is bracketed in the data.

2/ More than one op amp failed this parameter. The number of failures is shown next.

3/ No op amp meets the spec.

Table 3-11. Device type 01 (LM148) static test data at 125°C

Parameter Symbol	Voltages		Data (Sample Size = 56)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	V_{CM}	Low	High	$\bar{X}$	σ	$\%(\pm 2\sigma)$	$\%(\pm 3\sigma)$	Min	Max		
V_{IO}	20	15	-.64	(2.5)	1.19	1.66	98.21	98.21	-6	6	mV	1/ I2.3
	20	-15	-.974	1.06	.694	.693	96.43	100				
	20	0	-.850	2.15	.822	.703	96.43	100				
	5	0	-.303	2.67	1.28	.725	96.43	100				
I_I	20	15	-5.00	8.75	.752	2.22	96.43	98.21	-75	75	nA	
	20	-15	-3.08	8.6	.850	1.95	96.43	98.21				
	20	0	-3.00	9.15	.841	2.05	98.21	98.21				
	5	0	-2.75	6.75	1.23	1.73	96.43	98.21				
$+I_{IB}$	20	15	-5.15	34.33	8.70	8.64	98.21	100	1	325	nA	2/ I3/56
	20	-15	10.75	48.98	20.22	6.98	94.65	98.21				
	20	0	7.50	42.5	16.35	6.57	96.43	98.21				
	5	0	4.55	26.75	10.60	4.19	96.43	98.21				
$-I_{IB}$	20	15	-7.25	26.0	8.94	9.00	100	100	1	325	nA	2/ I2/56
	20	-15	9.20	39.5	19.60	7.08	94.64	100				
	20	0	5.00	33.0	15.9	6.72	96.43	100				
	5	0	.250	20.6	7.69	4.12	96.43	98.21				
+PSRR	20		-19.2	( )	-.198	18.66	98.21	98.21	-100	100	uV/V	1/133.1
-PSRR	20		-27.8	-3.75	-14.5	4.91	94.64	100	-100	100	uV/V	
CMR	20	±15	(95.39)	129.5	100.7	6.52	96.43	96.43	76	-	dB	1/67.8
$I_{OS(+)}$	15	0	-19.45	-13.6	-16.42	1.76	100	100	-55	-	mA	
$I_{OS(-)}$	15	0	6.52	9.60	7.86	.889	100	100	-	55	mA	
I_{CC}	20	0	-2.17	-1.65	-1.93	.160	100	100	-	4.5	mA	
	15	0	-1.96	-1.50	-1.75	.142	100	100	-	3.6		

Table 3-11. Device type 01 (LM148) static test data at 125°C (Continued)

Parameter Symbol	Voltages ±VCC	R_L	Data (Sample Size = 55) Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Spec. Limits Min	Max	Units	Notes
$V_{OP}(+)$	20	10K	19.25	19.30	19.28	.024	100	100	+16	-	V	
$V_{OP}(-)$	20	10K	-18.2	-17.95	-18.1	.056	96.43	100	-	-16	V	
$V_{OP}(+)$	20	2K	17.75	17.85	17.76	.026	92.86	92.86	+15	-	V	
$V_{OP}(-)$	20	2K	-16.9	-14.25	-16.0	.918	100	100	-	-15	V	2/12/56
$A_{VS}(+)$	20	10K	-10.0K	9.00K	.819	4.6K	94.64	100	25	-	V/mV	
$A_{VS}(-)$	20	10K	-30.0K	9.00K	.506	5.15K	96.43	98.21	25	-	V/mV	
$A_{VS}(+)$	20	2K	-3.33K	9.00K	1.32K	2.71K	91.07	100	25	-	V/mV	
$A_{VS}(-)$	20	2K	1.293	10.0	3.62	2.31	94.64	100	25	-	V/mV	3/
A_{VS}	5	10K	-19.7	111.1	4.89	16.44	96.43	98.21	10	-	V/mV	
A_{VS}	5	2K	-26.3	20.9	1.51	4.58	96.43	96.43	10	-	V/mV	
A_{VS}											V/mV	
A_{VS}											V/mV	
$\frac{\Delta V_{IO}}{\Delta T}$	20		-2.69	11.2	4.98	3.02	96.43	100	-25	25	uV/°C	
$\frac{\Delta I_{IO}}{\Delta T}$	20		-12.75	72.5	32.2	23.46	100	100	-200	200	PA/°C	

Table 3-11. Device type 01 (LM148) static test data at 125°C (Continued)

NOTES:

1/ One op amp failed this parameter. The failed limit is shown after the note and the next inside limit is bracketed in the data.

2/ More than one op amp failed this parameter. The ratio of failures to samples is shown next.

3/ No op amp meets the spec.

Table 3-12. Device type 01 (LM148) dynamic test data

Parameter Symbol	Data @ 25°C N = 20						/110 Rec		Units
	Min	Max	$\bar{X}$	σ	$\bar{X}-3\sigma$	$\bar{X}+3\sigma$	Min	Max	
TR(t_r)	.21	.27	.23	.018	.176	.284	-	1	us
TR(OS)	11.7	12.5	11.67	.547	10.03	13.31	-	25	%
SR(+)	.50	.68	.60	.068	.396	.804	0.2	-	V/us
SR(-)	.42	.56	.494	.050	.344	.644	0.2	-	V/us
CS	106	144	125.6	13.8	84.2	167	80	-	dB
N1(BB)	5.66	10.6	9.37	1.81	3.94	14.8	-	15	uVrms
N1(PC)	<1	2.0					-	40	uVpk

Table 3-13. Device type 03 (4741) data versus recommended limits

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
V_{IO}	V_{CM} = +15V, -15V, 0V @ $V_{CC} = \pm 20V$ V_{CM} = 0V @ $V_{CC} = \pm 5V$	-55 25 125			(-4.1) -2.65 -3.11	(4.65) 2.02 2.52	-5 -3 -5	5 3 5	mV
$\frac{\Delta V_{IO}}{\Delta T}$	V_{CM} = 0	-55/25 25/125			(-24.5) -5.7	(16) 9.25	-20 -20	20 20	uV/dc
I_{IO}	(Same as for V_{IO})	-55 25 125			-96 -37.5 -21	57.3 20 13.85	-75 -30 -30	75 30 30	nA
$\frac{\Delta I_{IO}}{\Delta T}$	V_{CM} = 0	-55/25 25/125			-261 -70	722 205	-500 -200	500 200	PA/°C
$+I_{IB}$	(Same as for V_{IO})	-55 25 125			-266 -254 -200.8	0 -75.9 -29.4	-325 -200 -200	-1 -1 -1	nA
$-I_{IB}$	(Same as for V_{IO})	-55 25 125			-241 -231.5 -202	0 -74 -31.2	-325 -200 -200	-1 -1 -1	nA
+PSRR		-55 25 125			-24 -23 -26.9	1550 9.5 10.2	-100 -100 -100	100 100 100	uV/V
-PSRR		-55 25 125			-24 -16.6 -20	1550 16 20	-100 -100 -100	100 100 100	uV/V

Table 3-13. Device type 03 (4741) data versus recommended limits (Continued)

Parameter Symbol	Conditions	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
CMR		-55			65.1	160	76	-	dB
		25			97.5	160	76	-	
		125			95.2	141.6	76	-	
$I_{OS(+)}$	$V_{CC} = \pm 15V$	-55			-43.3	-11.6	-80	-	mA
		25			-56.6	-20.9	-80	-	
		125			-53.8	-12.8	-80	-	
$I_{OS(-)}$	$V_{CC} = \pm 15V$	-55			27.0	74.95	-	80	mA
		25			37.15	65.85	-	80	
		125			16.75	54.8	-	80	
I_{CC}	$V_{CC} = \pm 20V$	-55			3.28	5.71	-	13	mA
		25			2.91	4.93	-	11	
		125			2.36	4.1	-	11	
Icc	$V_{CC} = \pm 15V$	-55			3.22	5.61	-		mA
		25			2.87	4.90	-		
		125			2.32	4.09	-		
$V_{OP(+)}$	R_L = 10 KΩ $V_{CC} = \pm 20V$	-55	16	-	18.2	18.85	16	-	V
		25	16	-	18.45	19.0	16	-	
		125	16	-	18.65	19.1	16	-	
$V_{OP(-)}$	R_L = 10 KΩ $V_{CC} = \pm 20V$	-55	-	-16	-18.05	-18.75	-	-16	V
		25	-	-16	-18.4	-18.1	-	-16	
		125	-	-16	-18.6	-18.3	-	-16	
$V_{OP(+)}$	R_L = 2 KΩ V_{CC} = +20V	-55	15	-	15.1	17.75	15	-	V
		25	15	-	16.75	17.85	15	-	
		125	15	-	16.7	17.8	15	-	

Table 3-13. Device type 03 (4741) data versus recommended limits (Continued)

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
$V_{OP(-)}$	R_L = 2 K	-55	-	-15	-16.9	17.65	-	-15	V
		25	-	-15	-17.05	-16.2	-	-15	
		125	-	-15	-17.2	-16.2	-	-15	
$A_{VS(+)}$	R_L = 10 K	-55	25	-	-3.75K	15K	25	-	V/mV
		25	50	-	-30K	30K	50	-	
		125	25	-	-15K	30K	25	-	
$A_{VS(-)}$	R_L = 10 K	-55	25	-	-7.5K	9K	25	-	V/mV
		25	50	-	-1000	-250	50	-	
		125	25	-	-3K	-189	25	-	
$A_{VS(+)}$	R_L = 2 K	-55	25	-	-30K	9K	25	-	V/mV
		25	50	-	-5K	43K	50	-	
		125	25	-	-15K	30K	25	-	
$A_{VS(-)}$	R_L = 2 K	-55	25	-	16.39	9K	25	-	V/mV
		25	50	-	68.8	341	50	-	
		125	25	-	17.96	115.4	25	-	
A_{VS}	V_{CC} = ±5V, R_L = 10 K	-55	10	-	1.2	13.24	10	-	V/mV
		25	10	-	-333	8K	10	-	
		125	10	-	-1.6K	800	10	-	
A_{VS}	V_{CC} = ±5V, R_L = 2 K	-55	10	-	.845	4.72	10	-	V/mV
		25	10	-	-138.9	15.7	10	-	
		125	10	-	-1.14K	2K	10	-	

Table 3-14. Device type 03 (4741) static test data at -55°C

Parameter Symbol	Voltages ±VCC	Voltages VCM	Data (Sample Size = 80) Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Spec. Limits Min	Spec. Limits Max	Units	Notes
V_{IO}	20	15	(-3.4)	(4.65)	-4.31	2.08	96.25	97.50	-6	6	mV	1/14.3
	20	-15	(-3.4)	(4.30)	.128	3.49	93.75	95.00				2/5/80
	20	0	(-3.4)	(4.30)	.177	3.48	93.75	95.00				2/5/80
	5	0	(-4.1)	4.42	-.610	1.39	96.25	97.50				2/-8.5
I_{IO}	20	15	-96.0	50.3	-8.46	22.5	93.75	97.50	-150	150	nA	
	20	-15	-65.0	23.87	-6.19	12.03	91.25	97.50				
	20	0	-75.0	33.9	-6.94	15.41	91.25	98.75				
	5	0	-77.5	56.5	-6.60	21.9	92.50	97.50				
$+I_{IB}$	20	15	-266	0.0	-112	60.1	96.25	100	-400	-1	nA	
	20	-15	-156.3	0.0	-57.3	33.95	97.50	100				
	20	0	-195.3	0.0	-76.14	42.64	97.50	100				
	5	0	-262	-52.9	-103.1	51.9	95.00	98.75				
$-I_{IB}$	20	15	-241	0.0	-102.9	52.2	96.25	100	-400	-1	nA	
	20	-15	-120.8	0.0	-51.1	30.7	98.75	100				
	20	0	-159.5	0.0	-69.3	37.8	98.75	100				
	5	0	-207.0	-46.8	-96.0	44.7	96.25	100				
+PSRR	20		-24.0	1.55K	76.1	324.7	95.00	95.00	-100	100	uV/V	2/4/80
-PSRR	20		-23.0	1.55K	77.2	324.1	95.00	95.00	-100	100	uV/V	2/4/80
CMR	20	±15	65.1	160.0	113.1	13.87	93.75	95.00	76	-	dB	2/3/80
$I_{OS(+)}$	15	0	-43.3	-11.6	-26.4	5.33	92.50	98.75	-80	-	mA	
$I_{OS(-)}$	15	0	27.0	74.95	58.74	7.59	95.00	98.75	-	80	mA	
I_{CC}	20	0	-5.71	-3.28	-4.76	.553	95.00	100	-	13	mA	
	15	0	-5.67	-3.22	-4.72	.552	95.00	100	-			

Table 3-14. Device type 03 (4741) static test data at -55°C (Continued)

Parameter Symbol	Voltages		Data (Sample Size = 80)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	R_L	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
$V_{OP}(+)$	20	10K	18.2	18.85	18.76	.102	97.50	97.50	16	-	V	
$V_{OP}(-)$	20	10K	-18.05	18.75	-16.08	7.99	95.00	95.00	-	-16	V	2/4/80
$V_{OP}(+)$	20	2K	15.10	17.75	17.40	.403	98.75	98.75	15	-	V	
$V_{OP}(-)$	20	2K	-16.90	17.65	-14.87	7.48	95.00	95.00	-	-15	V	2/4/80
$A_{VS}(+)$	20	10K	-3.75K	15.0K	1.74K	3.03K	90.00	98.75	25	-	V/mV	
$A_{VS}(-)$	20	10K	-7.5K	9.0K	525.0	3.15K	88.75	100	25	-	V/mV	
$A_{VS}(+)$	20	2K	-30K	9.0K	256.5	4.03K	93.75	98.75	25	-	V/mV	
$A_{VS}(-)$	20	2K	16.39	9.0K	600.0	1.94K	95.00	95.00	25	-	V/mV	
A_{VS}	5	10K	1.20	13.24	2.08	1.85	95.00	95.00	10	-	V/mV	2/79/80
A_{VS}	5	2K	.845	4.72	1.24	.592	96.25	96.25	10	-	V/mV	3/
A_{VS}											V/mV	
A_{VS}											V/mV	
$\frac{\Delta V_{IO}}{\Delta T}$	20		(-24.5)	(16)	-8.06	42.73	95	95	-25	25	uV/°C	2/7/80
$\frac{\Delta I_{IO}}{\Delta T}$	20		-261.2	721.8	46.77	130.7	95	97.5	-1000	1000	PA/°C	

Table 3-14. Device type 03 (4741) static test data at -55°C (Continued)

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes and the next inside limit is bracketed ( ).

2/ More than one op amp failed to meet spec. The number of failures is shown next.

3/ No parameter meets the spec.

Table 3-15. Device type 03 (4741) static test data at 25°C

Parameter Symbol	Voltages		Data (Sample Size = 80)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	V_{CM}	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
V_{IO}	20	15	-2.65	2.01	-.479	.824	92.50	98.75	-5	5	mV	
	20	-15	-2.495	2.01	-.438	.814	92.50	98.75				
	20	0	-2.55	1.98	-.468	.813	92.50	98.75				
	5	0	-2.595	2.02	-.485	.810	92.50	98.75				
I_{IO}	20	15	-41.4	22.5	-3.85	10.17	92.50	98.75	-75	75	nA	
	20	-15	-17.62	9.75	-2.89	4.74	90.00	98.75				
	20	0	-24.7	13.5	-3.20	6.48	90.00	98.75				
	5	0	-37.5	20.0	-3.26	9.22	92.50	98.75				
$+I_{IB}$	20	15	-253.8	-75.9	-133	45.6	93.75	100	-250	-1	nA	2/1/80
	20	-15	-123.5	-36.8	-66.1	27.2	98.75	100				
	20	0	-164.8	-52.0	-89.5	32.7	95.00	100				
	5	0	-222	-66.1	-116.1	43.4	93.75	100				
$-I_{IB}$	20	15	(-231.5)	-74.0	-129.1	41.9	95.00	100	-250	-1	nA	1/253
	20	-15	-122.8	-33.5	-63.5	25.9	97.50	100				
	20	0	-163.0	-50.0	-86.4	30.6	95.00	100				
	5	0	-215.8	-63.7	-113.0	40.0	93.75	100				
+PSRR	20		-23.0	9.50	-.746	4.57	96.25	97.50	-100	100	uV/V	
-PSRR	20		-16.6	16.0	3.21	5.26	95.00	98.75	-100	100	uV/V	
CMR	20	± 15	97.5	160.0	114.5	11.63	93.75	97.50	76	-	dB	
$I_{OS(+)}$	15	0	-56.6	-20.9	-29.9	9.21	95.00	100	-80	-	mA	
$I_{OS(-)}$	15	0	37.15	65.85	49.2	7.55	95.00	100	-	80	mA	
I_{CC}	20	0	-4.93	-2.91	-4.17	.472	95.00	100	-	11	mA	
	15	0	-4.90	-2.87	-4.14	.473	95.00	100	-			

Table 3-15. Device type 03 (4741) static test data at 25°C (Continued)

Parameter Symbol	Voltages ±Vcc	Voltages R_L	Data (Sample Size = 80) Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Spec. Limits Min	Spec. Limits Max	Units	Notes
$V_{OP(+)}$	20	10K	18.45	19.0	18.88	.0883	98.75	98.75	16	-	V	
$V_{OP(-)}$	20	10K	-18.4	-18.1	-18.17	.0874	97.50	100	-	-16	V	
$V_{OP(+)}$	20	2K	16.75	17.85	17.46	.318	98.75	100	15	-	V	
$V_{OP(-)}$	20	2K	-17.0	-16.2	-16.7	.313	100	100	-	-15	V	
Avs(+)	20	10K	-30K	30K	.651	5.86K	97.50	97.50	50	-	V/mV	
Avs(-)	20	10K	-1K	-250	-442	137.3	92.50	98.75	50	-	V/mV	
Avs(+)	20	2K	-5K	48.9K	1.52K	5.52K	97.50	98.75	50	-	V/mV	
Avs(-)	20	2K	68.8	341	177	65.8	97.50	100	50	-	V/mV	
Avs	5	10K	-333	8K	94.4	910	98.75	98.75	10	-	V/mV	
Avs	5	2K	-138.9	15.7	.305	15.87	98.75	98.75	10	-	V/mV	
Avs											V/mV	
Avs											V/mV	
$\frac{\Delta V_{IO}}{\Delta T}$	20	$V_{CM}=0$	-124.3	66.6	-8.06	42.7	95.00	95.00	-25	25	mV/°C	2/ 7/80
$\frac{\Delta I_{IO}}{\Delta T}$	20	$V_{CM}=0$	-261.3	721.9	46.8	130.7	95.00	97.50	-500	500	PA/°C	

Table 3-15. Device type 03 (4741) static test data at 25°C (Continued)

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes and the next inside limit is bracketed ( ).

2/ More than one op amp failed to meet spec The number of failures is shown next.

3/ No parameter meets the spec.

Table 3-16. Device type 03 (4741) static test data at 125°C

Parameter Symbol	Voltages		Data (Sample Size = 80)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	V_{CM}	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
V_{IO}	20	15	-3.11	2.52	-.471	1.06	92.50	100	-6	6	mV	
	20	-15	-2.95	2.45	-.433	1.04	92.50	100				
	20	0	-2.97	2.45	-.471	1.04	92.50	100				
	5	0	-3.0	2.49	-.472	1.04	92.50	100				
I_{IO}	20	15	-21.0	13.85	.740	6.55	95.00	97.50	-150	150	nA	
	20	-15	-8.5	7.25	1.32	3.07	96.25	98.75				
	20	0	-12.53	9.25	1.10	4.12	97.50	98.75				
	5	0	-17.5	12.9	1.00	5.80	95.00	97.50				
$+I_{IB}$	20	15	-200.3	-75.0	-128	29.4	96.25	100	-1	-300	nA	
	20	-15	-86.6	-29.4	-53.3	18.1	100	100				
	20	0	-119.5	-47.67	-78.95	21.04	100	100				
	5	0	-167.8	-53.3	-108.7	27.5	97.50	100				
$-I_{IB}$	20	15	-202.3	-78.6	-129.3	27.15	97.50	100	-1	-300	nA	
	20	-15	-85.75	-31.25	-54.95	17.34	100	100				
	20	0	-119.8	-51.0	-80.2	19.8	100	100				
	5	0	-163.8	-68.1	-110.1	25.1	97.50	100				
+PSRR	20		-26.95	10.2	-1.49	5.08	96.25	97.50	-100	100	uV/V	
-PSRR	20		-20.05	20.0	3.48	6.55	95.00	98.75	-100	100	uV/V	
CMR	20	+15	95.2	141.6	111.6	9.65	95.00	98.75	76	-	dB	
$I_{OS(+)}$	15	0	-53.8	-12.8	-27.0	13.5	100	100	-80	-	mA	
$I_{OS(-)}$	15	0	16.75	54.8	32.8	13.2	100	100	-	80	mA	
I_{CC}	20	0	-4.1	-2.36	-3.42	.401	95	100	-	10	mA	
	15	0	-4.09	-2.32	-3.39	.406	95.00	100				

Table 3-16. Device type 03 (4741) static test data at 125°C (Continued)

Parameter Symbol	Voltages ±Vcc	Voltages R_L	Data (Sample Size = 80) Low	High	$\bar{X}$	σ	%(±2 σ)	%(±3 σ)	Spec. Limits Min	Spec. Limits Max	Units	Notes
$V_{OP}(+)$	20	10K	18.65	19.1	19.0	.098	98.75	98.75	16	-	V	
$V_{OP}(-)$	20	10K	-18.6	-18.3	-18.43	.089	100	100	-	16	V	
$V_{OP}(+)$	20	2K	16.7	17.8	17.3	.353	100	100	15	-	V	
$V_{OP}(-)$	20	2K	-17.2	-16.2	-16.7	.355	100	100	-	-15	V	
$A_{VS}(+)$	20	10K	-15K	30K	.647	6.1K	95.00	97.50	25	-	V/mV	
$A_{VS}(-)$	20	10K	-3K	-189	-.395	.387	97.50	97.50	25	-	V/mV	
$A_{VS}(+)$	20	2K	-15K	30K	498	4.87K	96.25	97.50	25	-	V/mV	
$A_{VS}(-)$	20	2K	17.96	115.4	53.3	22.1	95.00	100	25	-	V/mV	2/7/80
A_{VS}	5	10K	-1.6K	800.0	-34.5	256	95.00	96.25	10	-	V/mV	
A_{VS}	5	2K	-1.14K	2K	-15.1	280	96.25	97.50	10	-	V/mV	
A_{VS}											V/mV	
A_{VS}											V/mV	
$\frac{\Delta V_{IO}}{\Delta T}$	20	V_{CM}=0	-5.7	9.25	-.023	3.02	96.25	98.75	-25	25	mV/°C	
$\frac{\Delta I_{IO}}{\Delta T}$	20	V_{CM}=0	-70	205	43.0	38.1	92.50	98.75	-1000	1000	PA/°C	

Table 3-16. Device type 03 (4741) static test data at 125°C (Continued)

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes and the next inside limit is bracketed ( ).

2/ More than one op amp failed to meet spec. The number of failures is shown next.

3/ No parameter meets the spec.

Table 3-17. Device type 03 (4741) dynamic test data

Parameter Symbol	Data @ 25°C N = 19						/110 Rec		Units	Notes
	Min	Max	$\bar{X}$	σ	$\bar{X}-3\sigma$	$\bar{X}+3\sigma$	Min	Max		
TR(t_r)	.11	.12	.112	.0042	.0994	.1246	-	0.2	uS	
TR(OS)	19	24	21.64	1.469	17.23	26.05	-	25	%	
SR(+)	1.32	1.47	1.36	.053	1.201	1.519	0.8	-	V/uS	
SR(-)	1.32	1.47	1.36	.048	1.216	1.504	0.8	-	V/uS	
CS	108	124	115	4.66	101	129	80	-	dB	
N_1(BB)	2.12	8.50	4.13	2.126	-7.2	10.58	-	5	uVrms	
N_1(PC)	<1	18	3.32	3.97			-	50	uVpk	

Table 3-18. Device type 03 (4156) data versus recommended limits

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
V_{IO}	V_{CM} = +15V, -15V, 0V @ $V_{CC} = \pm 20V$ V_{CM} = 0V @ $V_{CC} = \pm 5V$	-55 25 125			-1.48 -1.485 -1.940	4.60 .3275 .4735	-5 -3 -5	5 3 5	mV
$\frac{\Delta V_{IO}}{\Delta T}$	V_{CM} = 0	-55/25 25/125			-4.69 -4.45	8.25 4.06	-20 -20	20 20	uV/°C
I_{IO}	(Same As for V_{IO})	-55 25 125			-45.4 -36.38 -19.07	18.43 10.85 5.60	-75 -30 -30	75 30 30	nA
$\frac{\Delta I_{IO}}{\Delta T}$	V_{CM} = 0	-55/25 25/125			-117.2 -29.3	97.8 116.3	-500 -200	500 200	PA/°C
$+I_{IB}$	(Same as for V_{IO})	-55 25 125			-284 -289.5 -223.4	-45.6 -52.3 -44.63	-325 -200 -200	-1 -1 -1	nA
$-I_{IB}$	(Same as for V_{IO})	-55 25 125			-245 -260.0 -213.8	-40.6 -51.36 -44.8	-325 -200 -200	-1 -1 -1	nA
+PSRR		-55 25 125			-5.85 -12.05 -16.4	10.9 8.71 7.70	-100 -100 -100	100 100 100	uV/V
-PSRR		-55 25 125			-4.65 -8.25 -10.5	10.0 10.16 9.90	-100 -100 -100	100 100 100	uV/V

Table 3-18. Device type 03 (4156) data versus recommended limits (Continued)

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
CMR		-55			101.2	160.0	76	-	
		25			100.3	160.0	76	-	dB
		125			97.6	160	76	-	
$I_{OS(-)}$	$V_{CC} = \pm 15V$	-55			-28.9	-20.9	-80	-	
		25			-24.6	-21.0	-80	-	mA
		125			-15.9	-13.0	-80	-	
$I_{OS(-)}$	$V_{CC} = \pm 15V$	-55			48.35	62.05	-	80	
		25			36.8	46.75	-	80	mA
		125			16.8	22.3	-	80	
I_{CC}	$V_{CC} = \pm 20V$	-55			-5.57	-3.33			
		25			-4.91	-2.95			mA
		125			-3.92	-2.40			
I_{CC}	$V_{CC} = \pm 15V$	-55			-5.52	-3.27	-	13	
		25			-4.86	-2.91	-	11	mA
		125			-3.87	-2.36	-	11	
$V_{OP(+)}$	R_L = 10 K	-55	16	-	18.8	18.85	16	-	
		25	16	-	18.95	19.00	16	-	V
		125	16	-	19.0	19.1	16	-	
$V_{OP(-)}$	R_L = 10 K	-55	-	-16	-18.1	-17.95	-	-16	
		25	-	-16	-18.4	-18.2	-	-16	V
		125	-	-16	-18.6	-18.5	-	-16	
$V_{OP(+)}$	R_L = 2 K	-55	15	-	17.65	17.75	15	-	
		25	15	-	17.75	17.80	15	-	V
		125	15	-	17.5	17.75	15	-	

Table 3-18. Device type 03 (4156) data versus recommended limits (Continued)

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GECS Data Range Min	GECS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
$V_{OP}(-)$	R_L = 2 K	-55	-	-15	-16.9	-16.8	-	-15	V
		25	-	-15	-17.1	-16.95	-	-15	
		125	-	-15	-17.1	-16.9	-	-15	
$A_{VS}(+)$	R_L = 10 K	-55	25	-	-7.5K	9.0K	25	-	V/mV
		25	50	-	-30K	9.0K	50	-	
		125	25	-	-15K	30K	25	-	
$A_{VS}(-)$	R_L = 10 K	-55	25	-	-3.0K	9.0K	25	-	V/mV
		25	50	-	-625	-270	50	-	
		125	25	-	-1.25K	-254	25	-	
$A_{VS}(+)$	R_L = 2 K	-55	25	-	-2.7K	1.16K	25	-	V/mV
		25	50	-	-15K	15K	50	-	
		125	25	-	-15K	15K	25	-	
$A_{VS}(-)$	R_L = 2 K	-55	25	-	136	652	25	-	V/mV
		25	50	-	155	375	50	-	
		125	25	-	21.4	61.5	25	-	
A_{VS}	$V_{CC} = \pm 5V$, R_L = 15 K	-55	10	-	1.26	2.40	10	-	V/mV
		25	10	-	-178	6.77	10	-	
		125	10	-	-8K	1.6K	10	-	
A_{VS}	$V_{CC} = \pm 5V$, R_L = 2 K	-55	10	-	.871	1.37	10	-	V/mV
		25	10	-	1.35	26.6	10	-	
		125	10	-	-276	9.72	10	-	

Table 3-19. Device type 03 (4156) static test data at -55°C

Parameter Symbol	Voltages $\pm V_{CC}$	Voltages V_{CM}	Data (Sample Size = 40) Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Spec. Limits Min	Spec. Limits Max	Units	Notes
V_{IO}	20	15	-1.22	-.0088	-.648	.314	97.50	100	-6	6	mV	
	20	-15	-1.48	-.0104	-.671	.331	97.50	100				
	20	0	-1.35	4.60	-.666	.324	95.00	100				
	5	0	-1.33	-.147	-.687	.308	97.50	100				
I_{IO}	20	15	-45.4	18.43	-4.61	10.99	92.50	97.50	-150	150	nA	
	20	-15	-19.88	7.65	-3.35	5.52	95.00	100				
	20	0	-27.38	10.88	-3.92	7.12	92.50	97.50				
	5	0	-39.13	15.38	-3.96	9.94	95.00	97.50				
$+I_{IB}$	20	15	-284	-78.28	-145.7	65.28	97.50	100	-400	-1	nA	
	20	-15	-125.5	-45.6	-79.6	30.0	100	100				
	20	0	-172.4	-58.7	-102.4	41.3	100	100				
	5	0	-239	-70.6	-130.3	57.6	100	100				
$-I_{IB}$	20	15	-245	-73.2	-141.4	64.0	100	100	-400	-1	nA	
	20	-15	-126	-40.6	-76.4	30.1	100	100				
	20	0	-163	-53.2	-98.6	40.9	100	100				
	5	0	-215	-67.0	-126.1	56.1	100	100				
+PSRR	20		-5.85	10.9	1.81	4.05	97.50	100	-100	100	uV/V	
-PSRR	20		-4.65	10.0	2.97	3.70	97.50	100	-100	100	uV/V	
CMR	20	±15	101.2	160.0	121.9	12.33	97.50	97.50	76	-	dB	
$I_{OS(+)}$	15	0	-28.9	-20.9	-26.87	1.686	92.50	97.50	-80	-	mA	
$I_{OS(-)}$	15	0	48.35	62.05	55.64	3.27	92.50	100	-	80	mA	
I_{CC}	20	0	-5.57	-3.33	-4.69	.567	90.00	100	-	13	mA	
	15	0	-5.52	-3.27	-4.64	.573	90.00	100	-			

Table 3-19. Device type 03 (4156) static test data at -55°C (Continued)

Parameter Symbol	Voltages ±VCC	R_T	Data (Sample Size = 40) Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Spec. Limits Min	Max	Units	Notes
$V_{OP}(+)$	20	10K	18.8	18.85	18.825	.0253	100	100	16	-	V	
$V_{OP}(-)$	20	10K	-18.05	-17.95	-17.98	.0276	97.50	100	-	-16	V	
$V_{OP}(+)$	20	2K	17.65	17.75	17.72	.035	100	100	15	-	V	
$V_{OP}(-)$	20	2K	-16.9	-16.8	-16.95	.0202	82.50	100	-	-15	V	
$A_{VS}(+)$	20	10K	-7.50K	9.00K	1.23K	3.97K	97.50	100	25	-	V/mV	
$A_{VS}(-)$	20	10K	-3.00K	9.00K	-501	1.604K	97.50	97.50	25	-	V/mV	
$A_{VS}(+)$	20	2K	-2.73K	1.158K	198.0	756	92.50	95.00	25	-	V/mV	
$A_{VS}(-)$	20	2K	136.4	652.2	293.7	115.7	97.50	97.50	25	-	V/mV	
A_{VS}	5	10K	1.256	2.400	1.647	.349	97.50	100	10	-	V/mV	3/
A_{VS}	5	2K	.971	1.367	1.146	.132	100	100	10	-	V/mV	3/
A_{VS}											V/mV	
A_{VS}											V/mV	
$\frac{\Delta V_{IO}}{\Delta T}$	20	V_{CM}=0	-4.69	8.25	2.33	2.904	95.00	100	-25	25	mV/°C	
$\frac{\Delta I_{IO}}{\Delta T}$	20	V_{CM}=0	-117.2	97.8	11.13	35.23	95.00	97.50	-500	500	PA/°C	

Table 3-19. Device type 03 (4156) static test data at -55°C (Continued)

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes and the next inside limit is bracketed ( ).

2/ More than one op amp failed to meet spec. The number of failures is shown next.

3/ No parameter meets the spec.

Table 3-20. Device type 03 (4156) static test data at 25°C

Parameter Symbol	Voltages ±VCC	Voltages VCM	Data (Sample Size = 40) Low	High	$\bar{X}$	σ	%(±2 σ)	%(±3 σ)	Spec. Limits Min	Max	Units	Notes
V_{IO}	20	15	-1.485	.3275	-.438	.347	92.50	97.50	-5	5	mV	
	20	-15	-1.425	.2190	-.483	.3316	92.50	100				
	20	0	-1.480	.286	-.479	.338	92.50	100				
	5	0	-1.395	.213	-.448	.312	92.50	97.50				
I_{IO}	20	15	-36.38	10.85	-3.95	7.672	97.50	97.50	-75	75	nA	
	20	-15	-15.54	5.05	-2.478	3.721	90.00	97.50				
	20	0	-21.80	6.500	-3.028	4.882	95.00	97.50				
	5	0	-31.88	9.325	-3.647	6.884	97.50	97.50				
$+I_{IB}$	20	15	-289.5	-96.62	-164.3	62.78	100	100	-250	-1	nA	2/ 4/40
	20	-15	-132.2	-52.3	-87.43	28.59	100	100				
	20	0	-173.5	-69.20	-113.4	39.49	100	100				
	5	0	-244.6	-86.85	-147.1	56.26	100	100				
$-I_{IB}$	20	15	-260.0	-92.63	-160.9	61.84	100	100	-250	-1	nA	2/ 6/40
	20	-15	-133.2	-51.36	-85.22	28.64	100	100				
	20	0	-170.9	-67.25	-110.7	39.04	100	100				
	5	0	-225.11	-85.00	-143.2	54.82	100	100				
+PSRR	20		-12.95	8.710	-2.051	4.548	90.00	100	-100	100	uV/V	
-PSRR	20		-8.250	10.16	.512	4.26	95.00	100	-100	100	uV/V	
CMR	20	±15	100.31	160.0	118.9	11.87	95.00	97.50	76	-	dB	
$I_{OS(+)}$	15	0	-24.55	-21.00	-22.47	.9379	95.00	100	-80	-	mA	
$I_{OS(-)}$	15	0	36.80	46.75	42.23	2.73	97.50	100	-	80	mA	
I_{CC}	20	0	-4.905	-2.950	-4.076	.473	90.00	100	-	11	mA	
	15	0	-4.855	-2.905	-4.029	.477	90.00	100	-			

Table 3-20. Device type 03 (4156) static test data at 25°C (Continued)

Parameter Symbol	Voltages		Data (Sample Size = 40)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	R_L	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
$V_{OP}(+)$	20	10K	18.95	19.00	18.95	.00791	97.50	97.50	16	-	V	
$V_{OP}(-)$	20	10K	-18.35	-18.20	-18.24	.0316	97.50	97.50	-	-16	V	
$V_{OP}(+)$	20	2K	17.75	17.80	17.75	.0133	92.50	92.50	15	-	V	
$V_{OP}(-)$	20	2K	-17.05	-16.95	-16.99	.0320	100	100	-	-15	V	
$A_{VS}(+)$	20	10K	-30K	9K	-1.153K	5.34K	97.50	97.50	50	-	V/mV	
$A_{VS}(-)$	20	10K	-625	-270	-367	73.62	95.00	97.50	50	-	V/mV	
$A_{VS}(+)$	20	2K	-15.0K	15.0K	642.9	5.427K	92.50	100	50	-	V/mV	
$A_{VS}(-)$	20	2K	154.6	375.0	242.6	53.9	97.50	100	50	-	V/mV	
A_{VS}	5	10K	-177.8	(6.768)	-63.1	52.17	97.50	100	10	-	V/mV	2/13/40
A_{VS}	5	2K	(1.347)	26.60	3.172	4.55	95.00	97.50	10	-	V/mV	2/39/40
A_{VS}											V/mV	
A_{VS}											V/mV	

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes and the next inside limit is bracketed ( ).

2/ More than one op amp failed to meet spec. The number of failures is shown next.

3/ No parameter meets the spec.

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Table 3-21. Device type 03 (4156) static test data at 125°C

Parameter Symbol	Voltages		Data (Sample Size = 40)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	V_{CM}	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
V_{IO}	20	15	-1.940	.4735	-.365	.485	95.00	97.50	-6	6	mV	
	20	-15	-1.84	.299	-.4119	.456	95.00	97.50				
	20	0	-1.925	.4010	-.4037	.4691	95.00	97.50				
	5	0	-1.845	.388	-.342	.454	95.00	97.50				
I_{IO}	20	15	-19.07	5.60	-.939	4.05	95.00	97.50	-150	150	nA	
	20	-15	-6.775	3.750	-.0731	2.167	95.00	97.50				
	20	0	-10.175	3.750	-.481	2.722	95.00	97.50				
	5	0	-16.72	4.55	-1.184	3.905	95.00	97.50				
$-I_{IB}$	20	15	-223.4	-96.1	-146.9	39.32	100	100	-1	-300	nA	
	20	-15	-100.3	-44.63	-68.1	17.29	100	100				
	20	0	-135.5	-63.7	-94.1	23.80	100	100				
	5	0	-181	-84.83	-127.2	34.6	100	100				
$-I_{IB}$	20	15	-213.8	-94.4	-146.9	39.0	100	100	-1	-300	nA	
	20	-15	-99.00	-44.80	-68.29	17.16	100	100				
	20	0	-133.8	-65.52	-93.92	23.44	100	100				
	5	0	-178	-87.8	-125.7	33.62	100	100				
+PSRR	20		-16.4	7.70	-3.82	4.66	92.50	100	-100	100	uV/V	
-PSRR	20		-10.5	9.90	-1.24	5.057	97.50	100	-100	100	uV/V	
CMR	20	±15	97.59	160.0	116.4	13.02	97.50	97.50	76	-	dB	
$I_{OS(+)}$	15	0	-15.85	-13.0	-14.25	.688	95.00	100	-80	-	mA	
$I_{OS(-)}$	15	0	16.8	22.3	19.6	1.41	100	100	-	80	mA	
I_{CC}	20	0	-3.915	-2.395	-3.23	.365	90.00	100	-	10	mA	
	15	0	-3.865	-2.355	-3.186	.369	90.00	100				

Table 3-21. Device type 03 (4156) static test data at 125°C (Continued)

Parameter Symbol	Voltages		Data (Sample Size = 40)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	R_L	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
$V_{OP}(+)$	20	10K	19.0	19.1	19.075	.0277	97.50	100	16	-	V	
$V_{OP}(-)$	20	10K	-18.6	-18.45	-18.51	.0368	92.50	100	-	-16	V	
$V_{OP}(+)$	20	2K	17.5	17.75	17.62	.0531	95.00	100	15	-	V	
$V_{OP}(-)$	20	2K	-17.05	-16.9	-16.96	.0496	100	100	-	-15	V	
$A_{VS}(+)$	20	10K	-15.0K	30.0K	20.90	6.18K	95.00	100	25	-	V/mV	
$A_{VS}(-)$	20	10K	-1.25K	-254.2	-411	245.4	90.00	97.50	25	-	V/mV	
$A_{VS}(+)$	20	2K	-15K	15K	-80.9	4.53K	92.50	95.00	25	-	V/mV	
$A_{VS}(-)$	20	2K	21.40	61.40	32.81	10.50	95.00	100	25	-	V/mV	2/ I6/40
A_{VS}	5	10K	-8K	1.6K	-606	1.89K	95.00	95.00	10	-	V/mV	
A_{VS}	5	2K	-276	9.72	-73.8	68.66	95.00	100	10	-	V/mV	2/ I1/40
A_{VS}											V/mV	
A_{VS}											V/mV	
$\frac{\Delta V_{IO}}{\Delta T}$	20	V_{CM}=0	-4.45	4.06	.756	2.03	92.50	100	-25	25	mV/°C	
$\frac{\Delta I_{IO}}{\Delta T}$	20	V_{CM}=0	-29.25	116.25	25.47	27.07	95.00	97.50	-1000	1000	PA/°C	

Table 3-21. Device type 03 (4156) static test data at 125°C (Continued)

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes and the next inside limit is bracketed ( ).

2/ More than one op amp failed to meet spec. The number of failures is shown next.

3/ No parameter meets the spec.

Parameter Symbol	Data @ 25°C N = 20						/110 Rec		Units
	Min	Max	$\bar{X}$	σ	$\bar{X}-3\sigma$	$\bar{X}+3\sigma$	Min	Max	
TR(t_r)	.11	.13	.1235	.0067	.1034	.1436	-	0.2	us
TR(OS)	19.3	24.3	21.52	1.77	16.21	26.83	-	25	%
SR(+)	1.06	1.35	1.206	.086	.948	1.608	0.8	-	V/us
SR(-)	1.09	1.32	1.203	.078	.969	1.437	0.8	-	V/us
CS	103	113	107.4	3.72	96.24	118.56	80	-	dB
N1(BB)	2.83	4.24	2.90	.314	1.958	3.842	-	5	uVrms
N1(PC)	<1	6.0					-	50	uVpk

Table 3-22. Device type 03 (4156) dynamic test data

Table 3-23. Device type 04 (4136) data versus recommended limits

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
V_{IO}	V_{CM} = +15V, -15V, 0V @ V_{CC} = +20V V_{CM} = 0V @ V_{CC} = $\pm$5V	-55 25 125	-6 -5 -6	6 5 6	-2.13 -1.9 -5.9	(4.2) 4.58 5.14	-6 -5 -6	6 5 6	mV
$\frac{\Delta V_{TO}}{\Delta T}$	V_{CM} = 0	-55/25 25/125	-25 -25	25 25					uV/°C
I_{IO}	(Same as for V_{IO})	-55 25 125	-150 -75 -150	150 75 150	(-100) -68 -95.5	(114) (43) (135)	-150 -75 -75	150 75 75	nA
$\frac{\Delta I_{IO}}{\Delta T}$	V_{CM} = 0	-55/25 25/125	-1000 -500	1000 500					PA/°C
$+I_{IB}$	(Same as for V_{IO})	-55 25 125	-400 -250 -400	-1 -1 -1	-363 -200 -112.8	(153) (16) (4.5)	-400 -250 -250	-1 -1 -1	nA
$-I_{IB}$	(Same as for V_{IO})	-55 25 125	-400 -250 -400	-1 -1 -1	-226 -159 -104.7	(5.05) (-4) (-6)	-400 -250 -250	-1 -1 -1	nA
+PSRR		-55 25 125	-100 -100 -100	100 100 100	-26.8 -9.5 -35	12 18.5 26	-100 -100 -100	100 100 100	uV/V
-PSRR		-55 25 125	-100 -100 -100	100 100 100	-39.2 -50.5 -71.5	17 26.5 46.5	-100 -100 -100	100 100 100	uV/V

Table 3-23. Device type 04 (4136) data versus recommended limits (Continued)

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GECS Data Range Min	GECS Data Range Max	GECS Recomm. Min	GECS Recomm. Max	Units
CMR		-55	76	-	(81.25)	126.6	76	-	dB
		25	76	-	80.57	135.6	76	-	
		125	76	-	77.07	135.56	76	-	
$I_{OS(+)}$	$V_{CC} = \pm 15V$	-55	-80	-	-96	-31.4	-80	-	mA
		25	-80	-	-84	-39.3	-80	-	
		125	-80	-	-83.4	-35.2	-80	-	
$I_{OS(-)}$	$V_{CC} = \pm 15V$	-55	-	80	48.65	87.15	-	80	mA
		25	-	80	41.75	78.3	-	80	
		125	-	80	34.15	61.8	-	80	
I_{CC}	$V_{CC} = \pm 20V$	-55	-	13	3.32	9.46	-	13	mA
		25	-	11	2.99	8.64	-	11	
		125	-	10	2.51	8.86	-	10	
I_{CC}	$V_{CC} = \pm 15V$	-55	-	-	3.24	8.88	-	12	mA
		25	-	11	2.96	8.12	-	10	
		125	-	-	2.46	8.13	-	9	
$V_{OP(+)}$	$R_L = 10\ K\Omega$	-55	16	-	17.95	18.85	16	-	V
		25	16	-	18	18.95	16	-	
		125	16	-	17.5	19.1	16	-	
$V_{OP(-)}$	$R_L = 10\ K\Omega$	-55	-	-16	-18.0	-17.85	-	-16	V
		25	-	-16	-18.2	-18.15	-	-16	
		125	-	-16	-18.6	-18.4	-	-16	
$V_{OP(+)}$	$R_L = 2\ K\Omega$	-55	15	-	16.75	17.65	15	-	V
		25	15	-	16.75	17.7	15	-	
		125	15	-	15.9	17.55	15	-	

Table 3-23. Device type 04 (4136) data versus recommended limits (Continued)

Parameter Symbol	Conditions $V_{CC} = \pm 20V$	T_A °C	JC-41 Recomm. Min	JC-41 Recomm. Max	GEOS Data Range Min	GEOS Data Range Max	GEOS Recomm. Min	GEOS Recomm. Max	Units
$V_{OP}(-)$	R_L = 2 K Ω	-55	-	-15	-16.85	-16.55	-	-15	V
		25	-	-15	-16.95	-16.65	-	-15	
		125	-	-15	-16.9	-16.5	-	-15	
Avs(+)	R_L = 10 K Ω	-55	25	-	-30K	9K	25	-	V/mV
		25	50	-	-30K	30K	50	-	
		125	25	-	-20K	300K	25	-	
Avs(-)	R_L = 10 K Ω	-55	25	-	-6K	9K	25	-	V/mV
		25	50	-	-7.5K	9K	50	-	
		125	25	-	-5K	10K	25	-	
Avs(+)	R_L = 2 K Ω	-55	25	-	-7.5K	9K	25	-	V/mV
		25	50	-	-15K	27.3K	50	-	
		125	25	-	-3K	10K	25	-	
Avs(-)	R_L = 2 K Ω	-55	25	-	-3.75K	10K	25	-	V/mV
		25	50	-	-5K	9K	50	-	
		125	25	-	-750	769	25	-	
Avs	$V_{CC} = \pm 5V$ R_L = 10 K Ω	-55	10	-	1.36	2.53	10	-	V/mV
		25	10	-	-296	26.6	10	-	
		125	10	-	-16K	1.14K	10	-	
Avs	$V_{CC} = \pm 5K$ R_L = 2 K Ω	-55	10	-	1.30	1.376	10	-	V/mV
		25	10	-	1.31	2.28	10	-	
		125	10	-	-800	34.8	10	-	

Table 3-24. Device type 04 (4136) static test data at -55°C

Parameter Symbol	Voltages		Data (Sample Size = 80)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	V_{CM}	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
V_{IO}	20	15	-.78	3.17	1.37	1.025	95	100				
	20	-15	-2.13	(4.2)	1.30	1.96	98.75	98.75	-6	6	mV	1/14.3
	20	0	-1.28	3.19	1.195	1.104	96.25	100	100			
	5	0	-.64	3.29	1.48	1.00	96.25	100				
I_{IO}	20	15	(-100)	24.5	-20.87	32.55	97.50	98.75				1/228.7
	20	-15	-104	(114)	-8.6	28	96.25	96.25	-150	150	nA	1/163.2
	20	0	-148	12.7	-15.07	20.98	97.5	98.75				
	5	0	(-95)	23	-20	30.94	97.5	98.75				1/217
$+I_{IB}$	20	15	-363	-31	-75.9	57.4	96.25	97.50				
	20	-15	-184	(153)	-35.3	40.2	93.75	95.00	-400	-1	nA	2/6/80
	20	0	-235	-17.7	-52.69	40	96.25	97.50				
	5	0	-343	-26.2	-70.47	54.3	96.25	97.50				
$-I_{IB}$	20	15	-226	-13.7	-54.3	38.8	93.75	97.50				
	20	-15	-137	(5.05)	-26.6	24.18	95	97.5	-400	-1	nA	2/3/80
	20	0	-173	-7	-37.7	29.4	95	97.5				
	5	0	-207	-14.5	-50.9	35.9	94	97.5				
+PSRR	20		-26.8	12	-3.4	6.46	96.25	98.75	-100	100	uV/V	
-PSRR	20		-39.15	17	-11.87	11.69	95	100	-100	100	uV/V	
CMR	20	±15	(81.25)	126.6	102.6	9.14	95	98.75	76	-	dB	1/66.7
$I_{OS(+)}$	15	0	(-96)	-31.4	-73.5	12.2	97.5	97.5	-80	-	mA	2/18/80
$I_{OS(-)}$	15	0	48.65	(87.15)	75.17	7.65	98.75	98.75	-	80	mA	2/19/80
I_{CC}	20	0	-9.46	-3.32	-6.04	1.714	100	100	-	13	mA	
	15	0	-8.88	-3.24	-5.96	1.686	100	100	-			

Table 3-24. Device type 04 (4136) static test data at -55°C (Continued)

Parameter Symbol	Voltages ±Vcc	RL	Data (Sample Size = 80) Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Spec. Limits Min	Max	Units	Notes
$V_{OP(+)}$	20	10K	17.95	18.85	18.8	.097	98.75	98.75	16	-	V	
$V_{OP(-)}$	20	10K	-18.0	-17.85	-17.85	.034	98.75	100	-	-16	V	
$V_{OP(+)}$	20	2K	16.75	17.65	17.55	.105	98.75	98.75	15	-	V	
$V_{OP(-)}$	20	2K	-16.85	-16.55	-16.7	.067	96.25	100	-	-15	V	
$A_{VS(+)}$	20	10K	-30K	9K	2.04K	5.24K	98.75	98.75	25	-	V/mV	
$A_{VS(-)}$	20	10K	-6K	9K	405	3.42K	90	100	25	-	V/mV	
$A_{VS(+)}$	20	2K	-7.5K	9K	1.48K	3.6K	86.25	100	25	-	V/mV	
$A_{VS(-)}$	20	2K	-3.75K	10K	1.12K	3.0K	90	100	25	-	V/mV	
A_{VS}	5	10K	1.36	2.53	1.65	.247	96.25	98.75	10	-	V/mV	3/
A_{VS}	5	2K	1.00	1.376	1.135	.079	97.50	98.75	10	-	V/mV	3/
A_{VS}											V/mV	
A_{VS}											V/mV	

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes and the next inside limit is bracketed ( ).

2/ More than one op amp failed this spec. The number of failures is shown next.

3/ No parameter meets the spec.

Table 3-25. Device type 04 (4136) static test data at 25°C

Parameter Symbol	Voltages		Data (Sample Size = 72)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	V_{CM}	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
V_{IO}	20	15	-1.31	3.825	1.122	1.26	98.6	100				
	20	-15	-3.3	4.58	.821	1.62	94.4	100	-5	5	mV	
	20	0	-1.9	3.74	.927	1.36	95.8	100				
	5	0	-1.24	3.67	1.11	1.2	98.6	100				
I_{IO}	20	15	-68	7.25	-13.59	15.67	93.06	95.8				
	20	-15	-48.9	(43)	-1	13.32	97.22	97.22	-75	75	nA	2/ 2/72
	20	0	-46.2	6.92	-9.11	10.26	94.44	97.22				(256)
	5	0	-61.7	6.5	-11.97	14.77	93.06	95.83				
$+I_{IB}$	20	15	-200.5	-26.1	-62.0	29.79	94.44	98.61				
	20	-15	-106.5	(16.0)	-24.5	43.2	97.22	97.22	-250	-1	nA	2/ 2/72
	20	0	-141.5	-16.92	-42.4	21.2	95.83	98.61				246.5
	5	0	-185.8	-22.25	-55.96	28.38	94.44	98.61				
$-I_{IB}$	20	15	-159.3	-20.5	-47.4	21.3	97.22	97.22				
	20	-15	-91	(-4)	-23.5	14.66	95.83	98.61	-250	-1	nA	1/
	20	0	-118.2	-11.25	-33.3	16.38	97.22	97.22				(19.2)
	5	0	-148.2	-21.75	-45.18	19.67	97.22	97.22				
+PSRR	20		-9.55	18.4	2.25	5.53	95.83	100	-100	100	uV/V	
-PSRR	20		-50.5	26.5	-7.34	14.59	91.67	100	-100	100	uV/V	
CMR	20	±15	80.57	135.6	101.2	9.42	94.4	98.6	76	-	dB	
$I_{OS(+)}$	15	0	-84.4	-39.3	-65.2	9.0	90.28	100	-80	-	mA	2/6/72
$I_{OS(-)}$	15	0	41.75	78.3	64.3	5.50	93.06	98.61	-	80	mA	
I_{CC}	20	0	-8.64	-2.99	-5.56	1.6	100	100	-	11	mA	
	15	0	-8.12	-2.96	-5.49	1.57	100	100	-			

Table 3-25. Device type 04 (4136) static test data at 25°C (Continued)

Parameter Symbol	Voltages		Data (Sample Size = 72)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	R_L	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
$V_{OP(+)}$	20	10K	18	18.95	18.9	.111	98.61	98.61	16	-	V	
$V_{OP(-)}$	20	10K	-18.2	-18.15	-18.2	.033	100	100	-	-16	V	
$V_{OP(+)}$	20	2K	16.75	17.7	17.54	.121	98.61	98.61	15	-	V	
$V_{OP(-)}$	20	2K	-16.95	-16.65	-16.8	.058	93.06	100	-	-15	V	
$A_{VS(+)}$	20	10K	-30K	30K	2.3K	6.45K	97.22	97.22	50	-	V/mV	
$A_{VS(-)}$	20	10K	-7.5K	9K	608.8	3.67K	87.5	100	50	-	V/mV	
$A_{VS(+)}$	20	2K	-15K	27.3K	2.5K	5.53K	94.4	97.2	50	-	V/mV	
$A_{VS(-)}$	20	2K	-5K	9K	1.4K	3.2K	87.5	100	50	-	V/mV	
A_{VS}	5	10K	-296	26.6	-6.88	52.4	94.4	94.4	10	-	V/mV	2/
A_{VS}	5	2K	(1.31)	(2.28)	1.67	.272	97.22	100	10	-	V/mV	3/
A_{VS}											V/mV	
A_{VS}											V/mV	

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes. The next inside limit is bracketed.

2/ More than one op amp failed this spec. The number of failures is shown next.

3/ No op amp meets the spec.

Table 3-26. Device type 04 (4136) static test data at 125°C

Parameter Symbol	Voltages		Data (Sample Size = 72)						Spec. Limits		Units	Notes
	$\pm V_{CC}$	V_{CM}	Low	High	$\bar{X}$	σ	%($\pm 2\sigma$)	%($\pm 3\sigma$)	Min	Max		
V_{IO}	20	15	(-2.8)	4.295	.396	1.89	97.22	98.61	-6	6	mV	1/6.94
	20	-15	-5.9	5.14	63.6	2.33	94.44	98.61				I/7.21
	20	0	(-3.4)	4.28	.222	1.99	97.22	98.61				I/6.95
	5	0	(-2.8)	4.11	.374	1.77	97.22	98.61				I/6.10
I_{IO}	20	15	-49.9	11.0	-2.99	9.87	94.44	97.22	-150	150	nA	2/2/72
	20	-15	-95.5	(135.0)	10.23	57.84	97.22	97.22				(369.7)
	20	0	-30.75	42.5	.644	8.99	95.83	97.22				
	5	0	-43.9	11.25	-1.24	9.29	94.44	97.22				
$+I_{IB}$	20	15	-112.8	-20.21	-47	17.16	97.22	98.61	-400	-1	nA	2/4/72
	20	-15	-52.75	4.5	-6.96	60.22	97.22	97.22				2/2/72
	20	0	-76	(-.8)	-28.25	14.48	97.22	97.22				
	5	0	-104.9	-15.55	-41.24	16.79	97.22	98.61				
$-I_{IB}$	20	15	-104.7	-23.6	-43.12	13.8	97.22	98.61	-400	-1	nA	2/3/72
	20	-15	-60.75	(-6)	-17.66	15.9	97.22	98.61				(83)
	20	0	-78.25	-14.25	-28.83	11.3	97.22	98.61				
	5	0	-99	-23.25	-41.4	12.67	97.22	98.61				
+PSRR	20		-35	26	3.37	8.70	95.83	98.61	-100	100	uV/V	
-PSRR	20		-71.5	46.5	-6.066	21.02	91.67	98.61	-100	100	uV/V	
CMR	20	±15	77.07	135.56	77.07	135.56	95.83	100	76	-	dB	
$I_{OS(+)}$	15	0	-68.4	-35.25	-52.5	7.41	90.28	100	-80	-	mA	
$I_{OS(-)}$	15	0	34.15	61.8	49.27	4.44	93.06	98.61	-	80	mA	
I_{CC}	20	0	-8.86	-2.505	-5.109	1.837	97.22	100	-	10	mA	
	15	0	-8.13	-2.465	-5.00	1.77	100	100				

Table 3-26. Device type 04 (4136) static test data at 125°C (Continued)

Parameter Symbol	Voltages ±Vcc	RL	Data (Sample Size = 72) Low	High	$\bar{X}$	σ	%(±2σ)	%(±3σ)	Spec. Limits Min	Max	Units	Notes
$V_{OP(+)}$	20	10K	17.5	19.1	18.98	.180	98.61	98.61	16	-	V	
$V_{OP(-)}$	20	10K	-18.6	-18.4	-18.47	.036	90.28	98.61	-	-16	V	
$V_{OP(+)}$	20	2K	15.9	17.55	.249	.298	98.61	98.61	15	-	V	
$V_{OP(-)}$	20	2K	-16.9	-16.5	-16.67	.091	95.83	100	-	-15	V	
Avs(+)	20	10K	-20K	300K	5.3K	35.6K	98.61	98.61	25	-	V/mV	
Avs(-)	20	10K	-5K	10K	1.23K	3.57K	87.5	100	25	-	V/mV	
Avs(+)	20	2K	-3K	10K	1.74K	2.82K	88.89	100	25	-	V/mV	
Avs(-)	20	2K	-750	769	214	256	94.4	97.2	25	-	V/mV	
Avs	5	10K	-16K	1.14K	-254	1.9K	98.61	98.61	10	-	V/mV	
Avs	5	2K	-800	34.8	-21.3	100.9	98.61	98.61	10	-	V/mV	

NOTES:

1/ One op amp failed to meet spec. The failed limit is shown in the notes. The next inside limit is bracketed ( ).

2/ More than one op amp failed this spec. The number of failures is shown next.

3/ No op amp meets the spec.

Table 3-27. Device type 04 (4136) dynamic test data

Parameter Symbol	Data @ 25°C N = 20						/110 Rec.		Units	Notes
	Min	Max	$\bar{X}$	σ	$\bar{X}-3\sigma$	$\bar{X}+3\sigma$	Min	Max		
TR(t_r)	.18	.27	.1945	.0258	.117	.272	-	0.3	uS	
TR(OS)	29.2	35	31.9	2.17	25.39	38.41	-	25	%	1/
SR(+)	.83	1.25	1.145	.099	.848	1.442	0.6	-	V/uS	
SR(-)	1.04	1.32	1.211	.075	.986	1.436	0.6	-	V/uS	
CS	115	132	122.8	4.93	108	137.6	80	-	dB	
N_1(BB)	1.77	4.95	2.53	.691	.46	4.60	-	5	uVrms	
N_1(PC)	<1	5					-	50	uVpk	

NOTE:

1/ These failures were caused by fixture parasitics. The 4136 has an extra conversion DIP which changes its pin-out to be the same as for the other op amps.

Figure No.	Curve Tracer Display	Device Type	Comm. Type
3-10	Offset Voltage vs Supply Voltage	01	LM148
3-11	$+I_{IB}$ Current vs Common Mode Voltage	01	LM148
3-12	$-I_{IB}$ Current vs Common Mode Voltage	01	LM148
3-13	Common Mode Rejection	01	LM148
3-14	Power Supply Rejection	01	LM148
3-15	I_{CC} Current vs V_{CC} Voltage	01	LM148
3-16	AVS Gain vs Loading @ $+V_{CC}$ = +15V	01	LM148
3-17	AVS Gain vs Loading @ $\pm V_{CC}$ = $\pm$5V	01	LM148
3-18	Offset Voltage of 10 Devices	01	LM148
3-19	AVS Gain @ $+V_{CC}$ = +5V, R_L = 50KΩ	01	LM148
3-20	AVS Gain @ $\pm V_{CC}$ = $\pm$5V, R_L = 2KΩ	01	LM148
3-21	Common Mode Rejection of 8 Devices	01	LM148
3-22	Power Supply Rejection of 4 Devices	01	LM148
3-23	Supply Current for 5 Devices	01	LM148
3-24	Offset Voltage of 10 Devices	05	LM124
3-25	AVS Gain @ V_{CC} = 5V, R_L = 50KΩ	05	LM124
3-26	AVS Gain @ $\pm V_{CC}$ = $\pm$5V, R_L = 50KΩ	05	LM124
3-27	Effect of Feedback on AVS Gain	05	LM124
3-28	Closed Loop Gain vs Loading	05	LM124
3-29	AVS Open Loop Gain	05	LM124
3-30	AVS Gain Spread of 10 Devices	-	3503 (E)
3-31	AVS Gain Spread of 10 Devices	-	3503 (B)
3-32	Typical AVS of 10 Devices	-	3503 (F)

Table 3-28. Curve tracer display directory

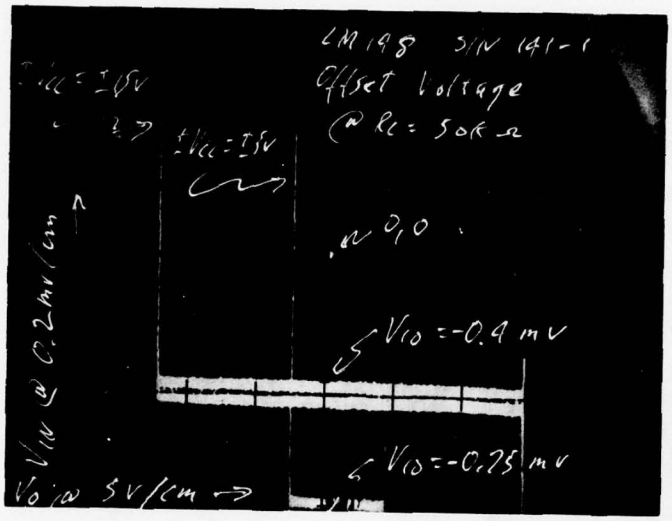

Figure 3-10.
LM148 S/N 141-1
Input Offset Voltage
for Different V_{CC}'s
($\pm V_{CC}$ = ±15V, ±5V)
V_{IO} @ 0.2 mV/cm ↑
V_O @ 5V/cm →
V_{IO} = -0.4 mV @
$\pm V_{CC}$ = ±15V
V_{IO} = -0.75 mV @
$\pm V_{CC}$ = ±5V

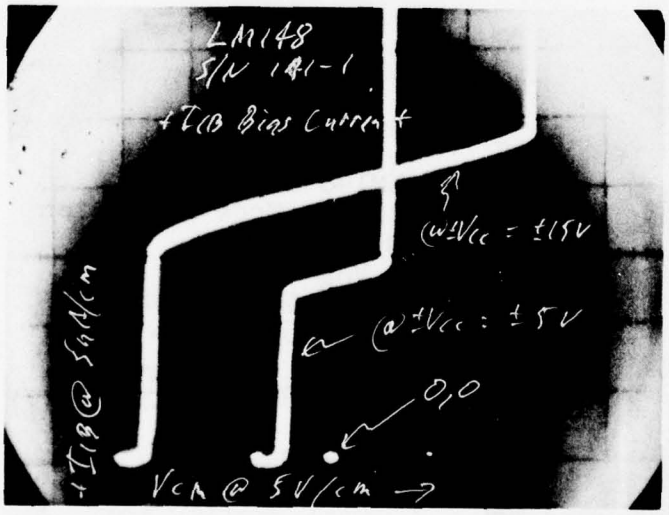

Figure 3-11.
LM148 S/N 141-1
Input Bias Current
for Different V_{CC}'s
($\pm V_{CC}$ = ±15V, ±5V)
$+I_{IB}$ @ 5 nA/cm ↑
V_{CM} @ 5 V/cm →
$+I_{IB}$ = 20 nA @
$\pm V_{CC}$ = ±15V
$+I_{IB}$ = 13 nA @
$\pm V_{CC}$ = ±5V

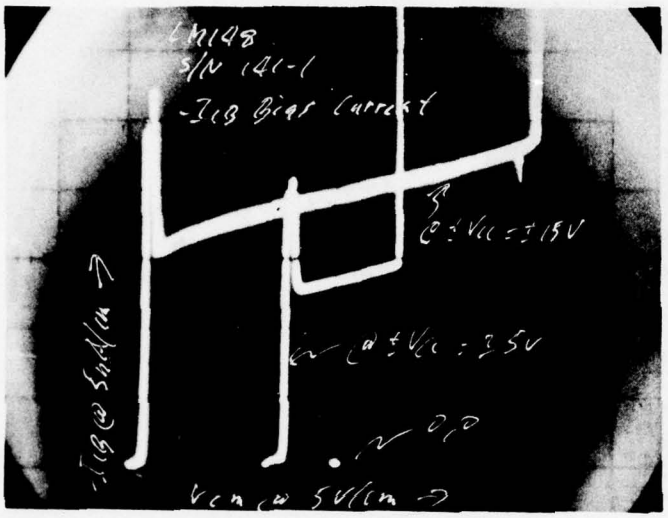

Figure 3-12.
LM148 S/N 141-1
Input Bias Current
for Different V_{CC}'s
($+V_{CC}$ = ±15V, +5V)
$-I_{IB}$ @ 5 nA/cm ↑
V_{CM} @ 5 V/cm →
$-I_{IB}$ = 19.5 nA @
$\pm V_{CC}$ = +15V
$-I_{IB}$ = 13 nA @
$\pm V_{CC}$ = ±5V

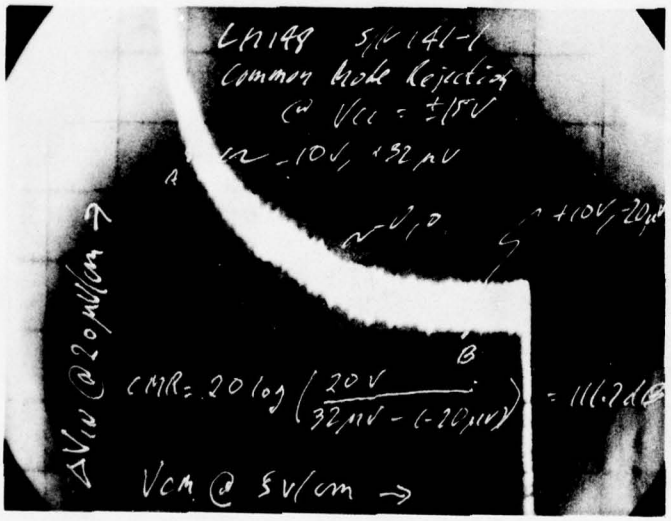

Figure 3-13.

LM148 S/N 141-1
Common Mode Rejection
@ V_{CC} = ±15V
V_{CM} = ±10V
ΔV_{IN} @ 20 uV/cm ↑
V_{CM} @ 5 V/cm →

$$CMR = 20 \log \frac{20V}{32\ uV-(-20\ uV)}$$

CMR = 111.7 dB

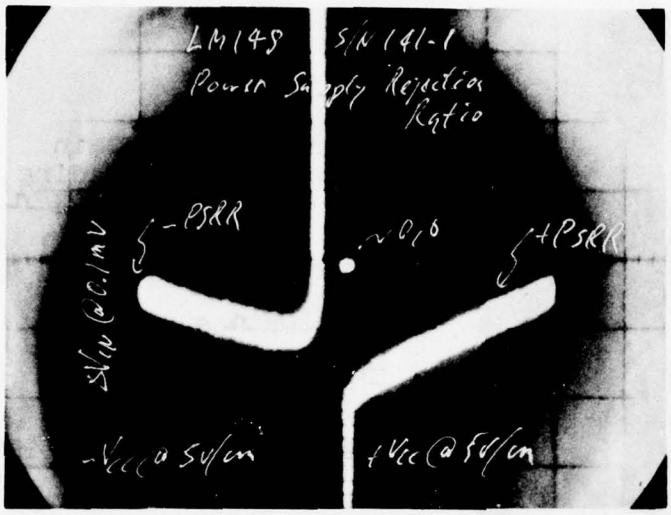

Figure 3-14.
LM148 S/N 141-1
Power Supply Rejection Ratio
+PSRR and -PSRR
@ V_{CC} = +15V
ΔV_{IN} @ 0.1 mV/cm ↑
ΔV_{CC} @ 5 V/cm →

$$+PSRR = \frac{.09\ mV}{10V} = 9\ uV/V$$

$$-PSRR = \frac{.06\ mV}{10V} = 6\ uV/V$$

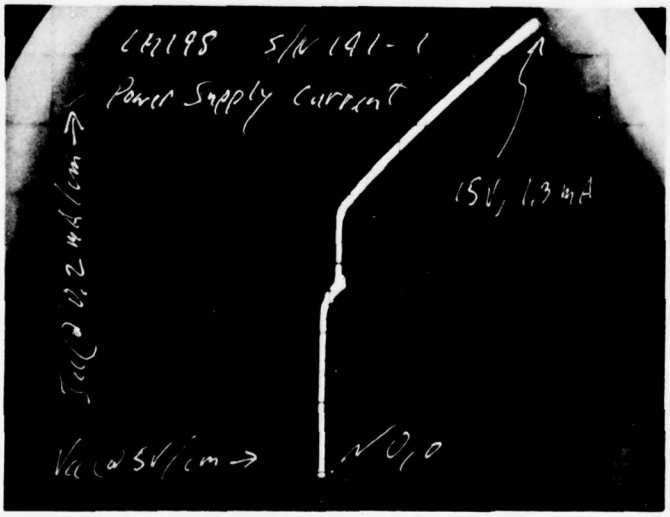

Figure 3-15.
LM148 S/N 141-1
Power Supply Current
@ V_{CC} = +15V
I_{CC} @ 0.2 mA/cm ↑
V_{CC} @ 5 V/cm →
I_{CC} = 1.3 mA @
$\pm V_{CC} = \pm 15V$

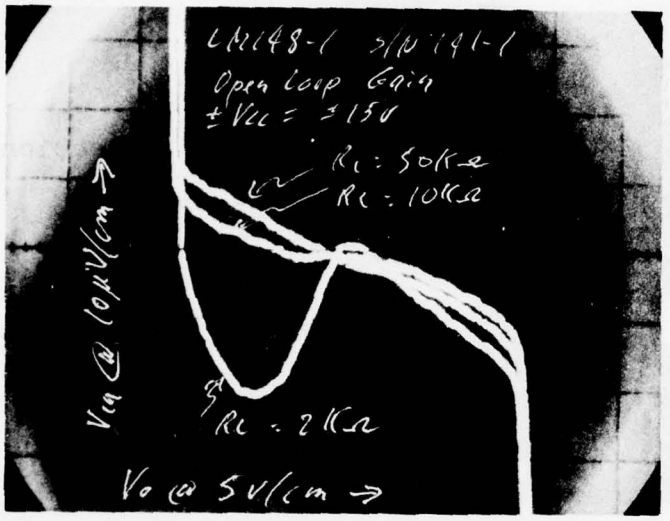

Figure 3-16.
LM148 S/N 141-1
Open Loop Voltage Gain
As A Function of Loading
@ $+V_{CC}$ = +15V, R_L = 2KΩ,
10KΩ, 50KΩ,
V_{IN} @ 10 uV/cm ↑
V_O @ 5 V/cm →
$+A_{VS}$ @ 10KΩ =

$$\frac{10V}{-8\ uV} = -1250\ V/mV$$

$-A_{VS}$ @ 10KΩ =

$$\frac{-10V}{6\ uV} = -1666\ V/mV$$

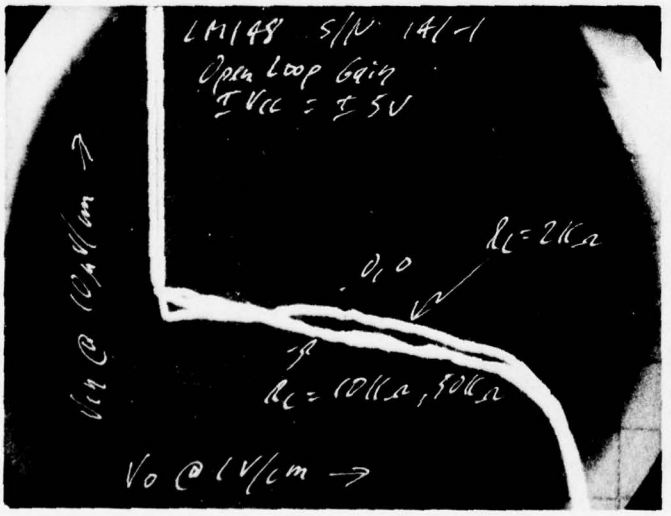

Figure 3-17.
LM148 S/N 141-1
Open Loop Voltage Gain
As A Function of Loading
@ $+V_{CC}$ = +5V, R_L = 2KΩ,
10KΩ, 50KΩ,
V_{IN} @ 10 uV/cm ↑
V_O @ 5V/cm →
A_{VS} @ 10KΩ =

$$\frac{4V}{8\ uV} = 500\ V/mV$$

A_{VS} @ 2KΩ =

$$\frac{4V}{5\ uV} = 800\ V/mV$$

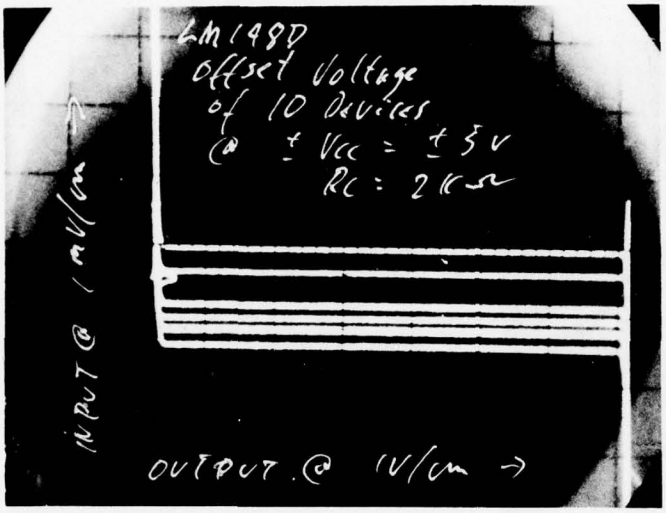

Figure 3-18.
LM148D
Offset Voltage
of 10 Devices
@ +VCC = +5V
$\overline{R_L}$ = 2K
Input @ 1 mV/cm
Output @ 1 V/cm →

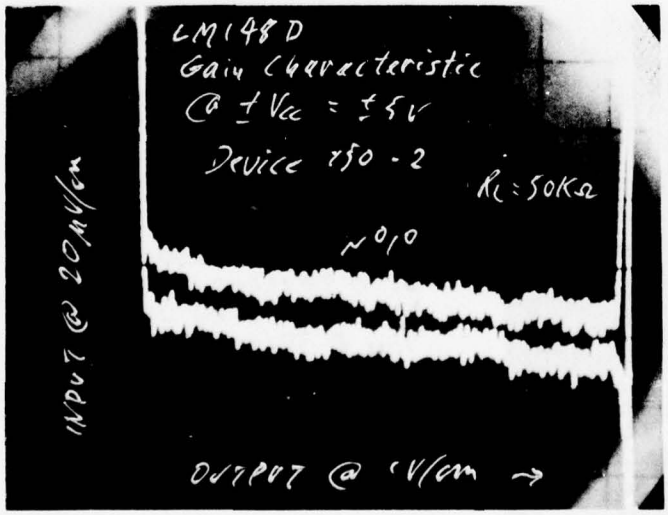

Figure 3-19.
LM148D
Gain Characteristic
@ +VCC = +5V
$\overline{R_L}$ = 50K
Input @ 20 uV/cm
Output @ 1 V/cm →

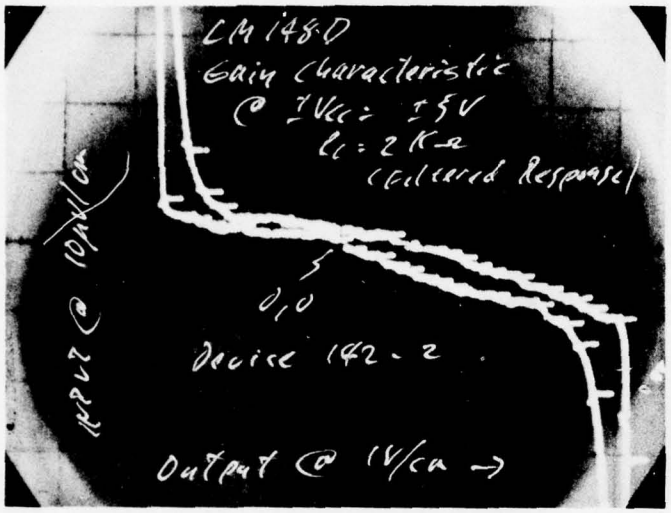

Figure 3-20.
LM148D
Gain Characteristic
@ $\pm V_{CC}$ = ±5V
R_L = 2KΩ
(Note that the locus is different depending on the direction being swept.)
Input @ 10 uV/cm ↑
Output @ 1 V/cm →

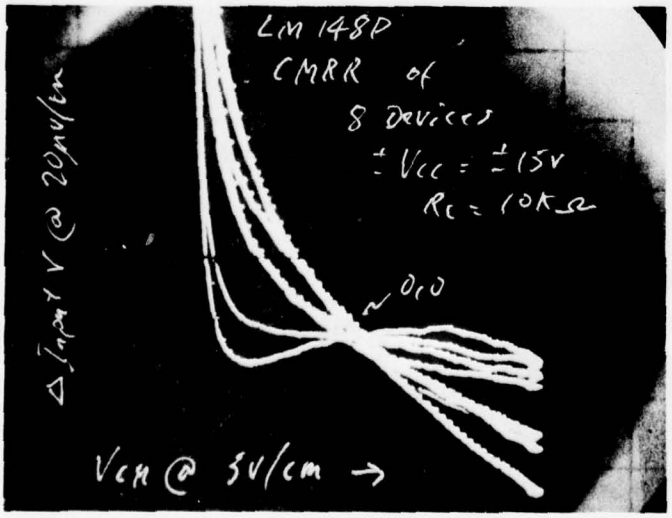

Figure 3-21.
LM148D
Common Mode
Rejection Ratio
of 8 Devices
ΔV Input @ 20 uV/cm ↑
V_{CM} @ 5V/cm →

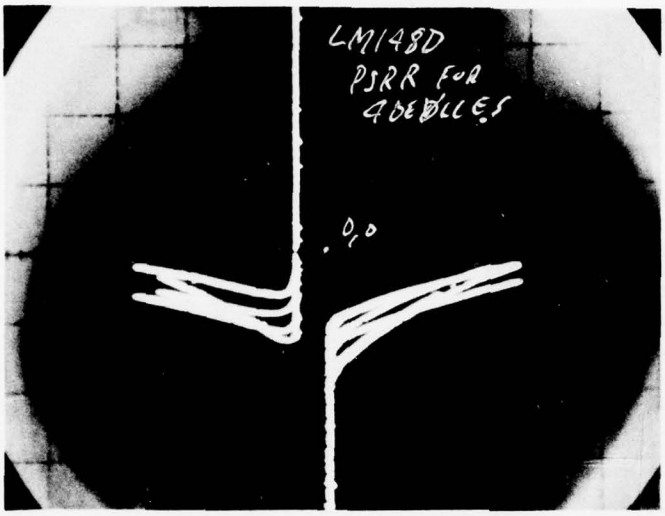

Figure 3-22.
LM148D
Power Supply
Rejection Ratio
of 4 Devices
△V Input @.2mV/cm↑
V @ 5 V/cm →

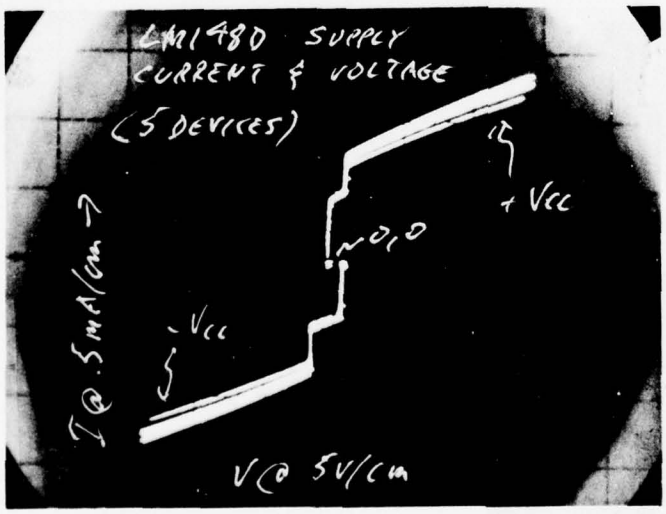

Figure 3-23.
LM148D
Supply Current
versus Voltage
of 5 Devices
I @ .5 mA/cm ↑
V @ 5 V/cm →

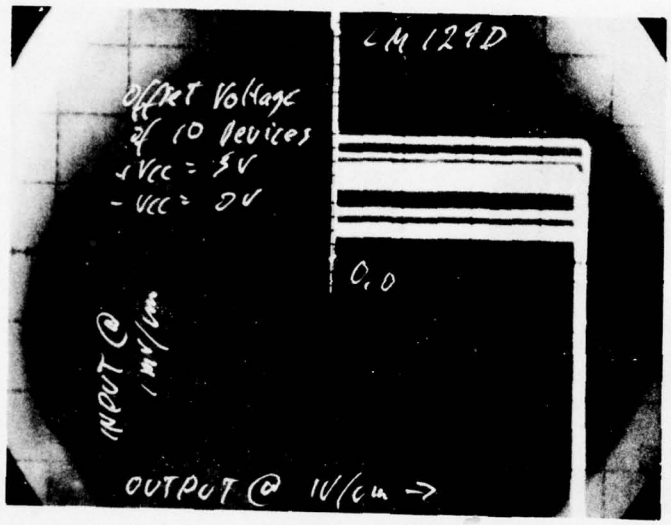

Figure 3-24.
LM124D
Offset Voltage
of 10 Devices
@ $+V_{CC}$ = 5V
$-V_{CC}$ = 0V
Input @ 1 mV/cm ↑
Output @ 1 V/cm →

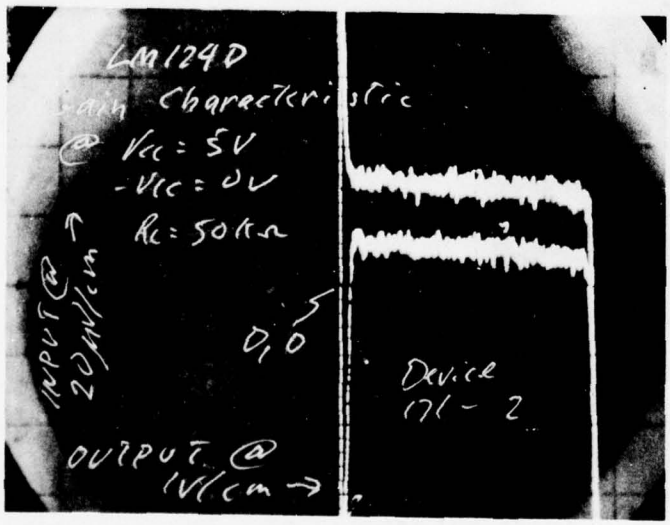

Figure 3-25.
LM124D
Gain Characteristic
@ V_{CC} = 5V
$-V_{CC}$ = 0V
R_L = 50KΩ
Input @ 20 uV/cm ↑
Output @ 1 V/cm →

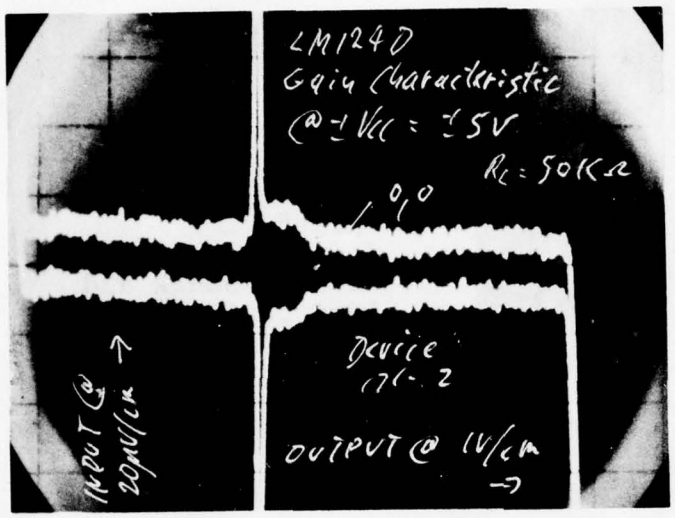

Figure 3-26.
LM124D
Gain Characteristic
@ $+V_{CC}$ = +5V
R_L = 50KΩ
(The characteristic becomes non-linear with increasing load)
Input @ 20 uV/cm ↑
Output @ 1 V/cm →

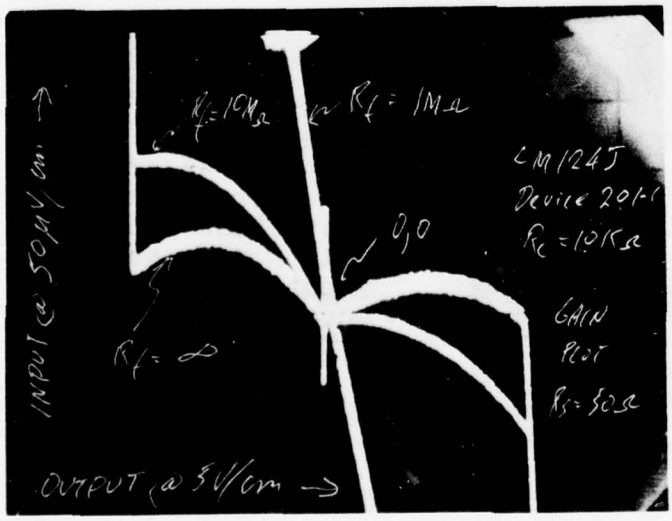

Figure 3-27.
LM124J
Gain Characteristic
(Note the effect of feedback on gain and its linearity.)
Input @ 50 uV/cm ↑
Output @ 5 V/cm →

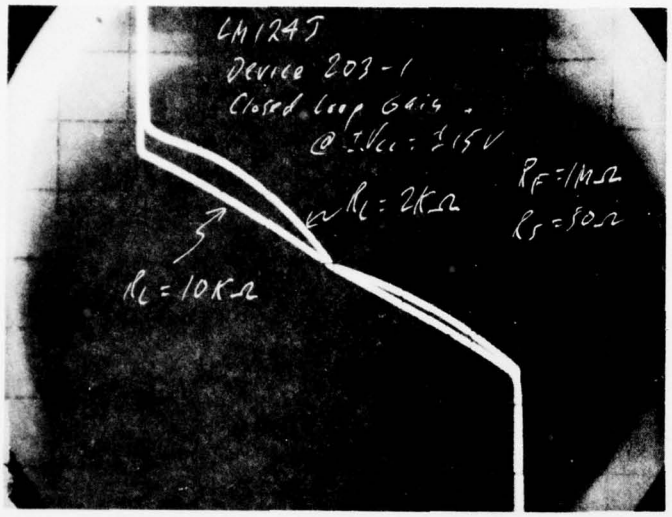

Figure 3-28.
LM1245
Gain Characteristic
with feedback and
load resistance.

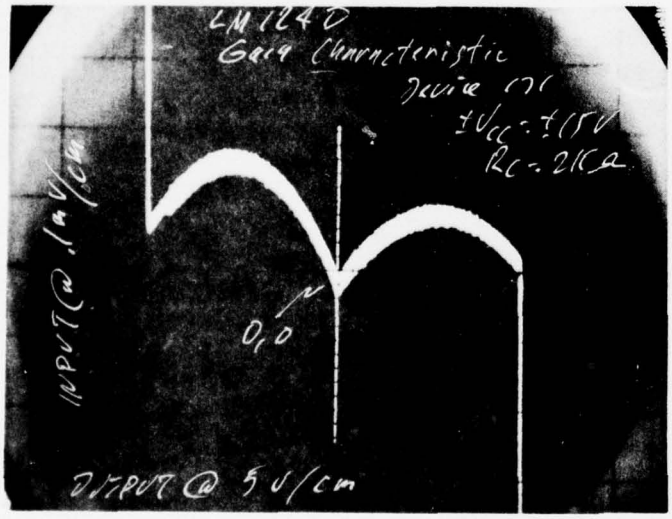

Figure 3-29.
LM124D
Gain Characteristic
(Note crossover
distortion and
gain non-linearity.)
Input @ .1 mV/cm ↑
Output @ 5 V/cm →

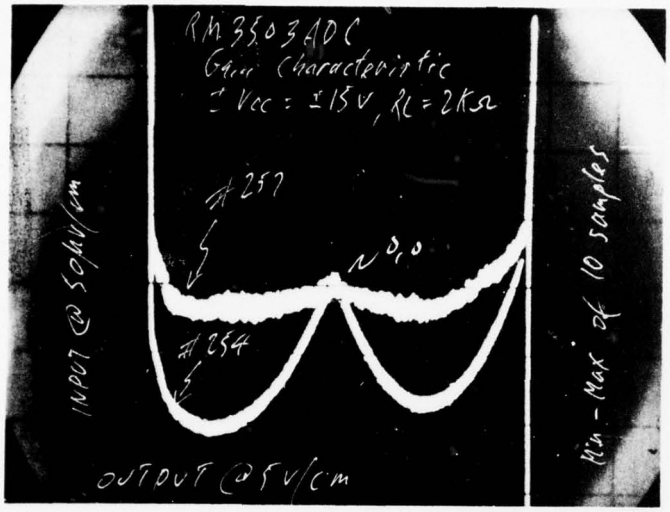

Figure 3-30.
RM3503ADC
Gain Characteristic
Input @ 50 uV/cm ↑
Output @ 5 V/cm →
(Minimum and maximum gains of 10 devices.)

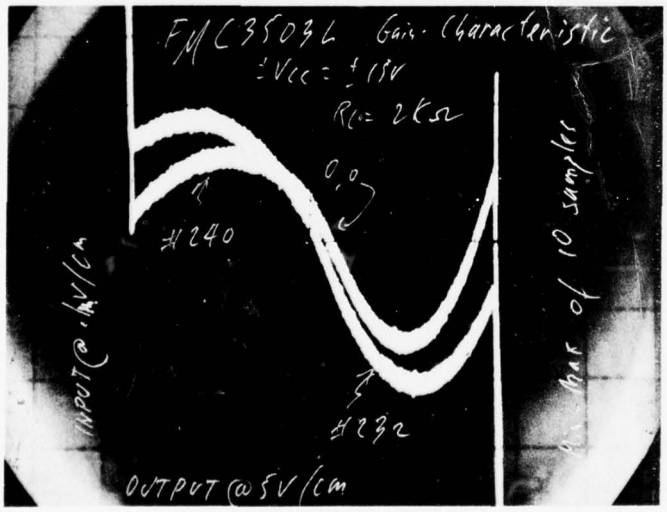

Figure 3-31.
MC3503L
Gain Characteristic
Input @ 0.1 mV/cm ↑
Output @ 5V/cm →

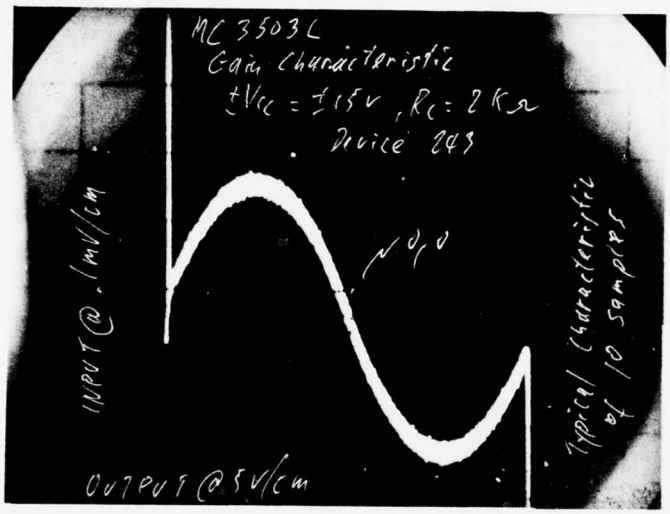

Figure 3-32.
MC3503L
Gain Characteristic
Input @ 0.1 mV/cm ↑
Output @ 5 V/cm →

SECTION IV

QUAD COMPARATORS

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SECTION IV

QUAD COMPARATORS

4.1 Background and Introduction

Quad comparators are very useful devices for circuit mechanizations involving multiple comparators. As with the quad operational amplifiers, increasing the device density results in more function per watt, but fewer options per function because of pin out restrictions. Quite often comparators are used to interface between linear and digital circuits. Since digital devices have higher function to package ratios than linear devices, the need for quad comparators is obvious.

The 139 was selected for characterization because it is popular among users and it is multiple sourced.

4.2 Description of Device Type

The 139 quad comparator consists of four independent voltage comparators with a common set of power terminals. For single power supply operation the recommended voltage range is from 5V to 30V. Dual supply operation is also possible. Each comparator has a differential front end with PNP transistor inputs.

Each output is the open collector of an NPN current sinking transistor. Because of pin out restrictions offset voltage adjustment and strobing are not available options. Electrical performance characteristics as proposed by the JC-41 Committee are shown in Table 4-1.

4.3 Discussion

The characterization effort to yield the procedures and limits of the future MIL-M-38510/112 quad comparator specification involves a number of phases. The starting point is recommended tests and limits from the joint industry JC-41 committee. There are 3 sources of data planned for verification of limits:

1. GEOS tests of purchased devices.
2. Manufacturer tests (performed by one source) of manufacturer-supplied devices, unmarked and serialized.
3. GEOS tests of samples from (2) above.

Trends and anomalies are being checked on a Tektronix 577 curve tracers with a 178 linear IC plug-in. Correlation of the difference data sources will assure realistic device limits.

Figure 4-1 shows the initial standard test circuit and conditions for the quad comparator with the exception of response times t_{RLH} and t_{RHL}. This same circuit applies to the S-3260 and the MIL-M-38510/112 specification. The 577 curve tracer test circuit cannot be used directly without first adding a 15 KΩ pull-up resistor and a .047 uf compensation capacitor for each comparator. These modifications are made on the plug-in card.

The 577 curve tracer test circuit deviates from the standard test circuit in at least two respects:

1. The output is programmally loaded to ground with 50 KΩ (min). (i.e. this load cannot be switched out.)

2. In the offset voltage mode R_s changes from 50 ohm to 550 ohm when the vertical sensitivity is switched from 0.5 mV/div to 1 mV/div.

Table 4-2 presents test conditions to be used with the figure 4-1 test circuit.

This task will be continued and completed on a future effort.

Table 4-1.

Electrical Performance

Proposed Voltage Comparator Specifications for 139

CONDITIONS: $-55°C < T_A < +125°C$ unless otherwise specified
$+5V \leq V^+ \leq +30V$ $-V=0V$ $R_L=15K$ $R_S=10K$

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Input Offset Voltage	V_{IO}	$V^+ = 30V$ $V_{CM} = 0, 28.5$ $V_{OUT} = 15V$ $T_A = 25°C$	-5	+5	
		$V^+ = 5V$ $V_{CM} = 0, 3.5V$ $V_{OUT} = 1.4V$ $T_A = 25°C$	-5	+5	mV
		$V^+ = +30V$ $V_{CM} = 0, 28V$ $V_{OUT} = 15V$ $T_A = -55°C$ & $T_A = 125°C$	-8	+8	mV
		$V^+ = 5V$ $V_{CM} = 0, 3V$ $V_{OUT} = 1.4V$ $T_A = 125°C$	-8	+8	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$V^+ = 30V$ $V_{CM} = 0$, $V_{OUT} = 15V$ $V_{CM} = 0$, $+25°C < T_A < +125°C$	-30	30	uV/°C
		$V^+ = 30V$ $V_{CM} = 0$, $V_{OUT} = 15V$ $V_{CM} = 0$, $-55°C \quad T_A \quad 25°C$	-30	30	uV/°C
Input Offset Current	I_{IO}	$V^+ = 30V$, $V_{CM} = 0, 28.5V$, $V_{OUT} = 15V$ $T_A = 25°C$	-25	25	nA
		$V^+ = 5V$ $V_{CM} = 0, 3.5V$, $V_{OUT} = 1.4V$ $T_A = 25°C$	-25	25	nA
		$V^+ = 30V$, $V_{CM} = 0, 28V$, $V_{OUT} = 15V$ $T_A = 125°C$	-25	25	nA
		$V^+ = 5V$, $V_{CM} = 0, 3V$ $V_{OUT} = 1.4V$ $T_A = 125°C$	-25	25	nA
		$V^+ = 30V$, $V_{CM} = 0, 28V$ $V_{OUT} = 15V$ $T_A = -55°C$	-100	100	nA
		$V^+ = 5V$ $V_{CM} = 0, 3V$ $V_{OUT} = 1.4V$, $T_A = -55°C$	-100	100	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	$V^+ = 30V$ $V_{CM} = 0$, $+25°C \quad T_A \quad +125°C$	-300	300	pA/°C
		$V^+ = 30V$ $V_{CM} = 0$, $-55°C \quad T_A \quad 25°C$	-600	600	pA/°C
Input Bias Current	I_{IB}	$V^+ = 30V$, $V_{CM} = 0, 28.5V$, $V_{OUT} = 15V$ $T_A = 25°C$	-100	-1	nA
		$V^+ = 5V$ $V_{CM} = 0, 3.5V$, $V_{OUT} = 1.4V$ $T_A = 25°C$	-100	-1	nA
		$V^+ = 30V$ $V_{CM} = 0, 28V$, $V_{OUT} = 15V$ $T_A = 125°C$	-100	-1	nA
		$V^+ = 5V$ $V_{CM} = 0, 3V$, $V_{OUT} = 1.4V$ $T_A = 125°C$	-100	-1	nA
		$V^+ = 30V$, $V_{CM} = 0, 28V$, $V_{OUT} = 15V$ $T_A = -55°C$	-300	-1	nA
		$V^+ = 5V$, $V_{CM} = 0, 3V$, $V_{OUT} = 1.4V$ $T_A = -55°C$	-300	-1	nA

Table 4-1.

Electrical Performance

Proposed Voltage Comparator Specifications for 139

CONDITIONS: $-55°C < T_A < +125°C$ unless otherwise specified
$+5V \leq V^+ \leq +30V$ $-V=0V$ $R_L=15K$ $R_S=10K$

CHARACTERISTICS	SYMBOL	CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Positive Supply Current	I_{CC+}	+V=5V I_O =0 -V=0V	T_A = 25°C		2	mA
			T_A = 125°C		2	
			T_A = -55°C		4	
		V^+ = 30V, I_O =0	T_A = 25°C		3	mA
			T_A = 125°C		3	
			T_A = -55°C		5	
Voltage Gain	$AV\pm$	Vc= +15V Vout = 10V Vout = 1 to 11V R_L = 15K	T_A = 25°C	50		V/mV
			T_A = -55°C	25		V/mV
			T_A = 125°C	25		V/mV
Response Time * Low to High Level	t_{RLH}	V_{IN} = 100mV, V_{OD} = 5mV, R_L = 5.1KΩ Vcc = 5V	T_A = 25°C		5	µS
Response Time * High to Low Level	t_{RHL}	V_{IN} = 100mV V_{OD} = 5mV, R_L = 5.1KΩ Vcc = 5V	T_A = 25°C		5	µS

* Sample Test Only

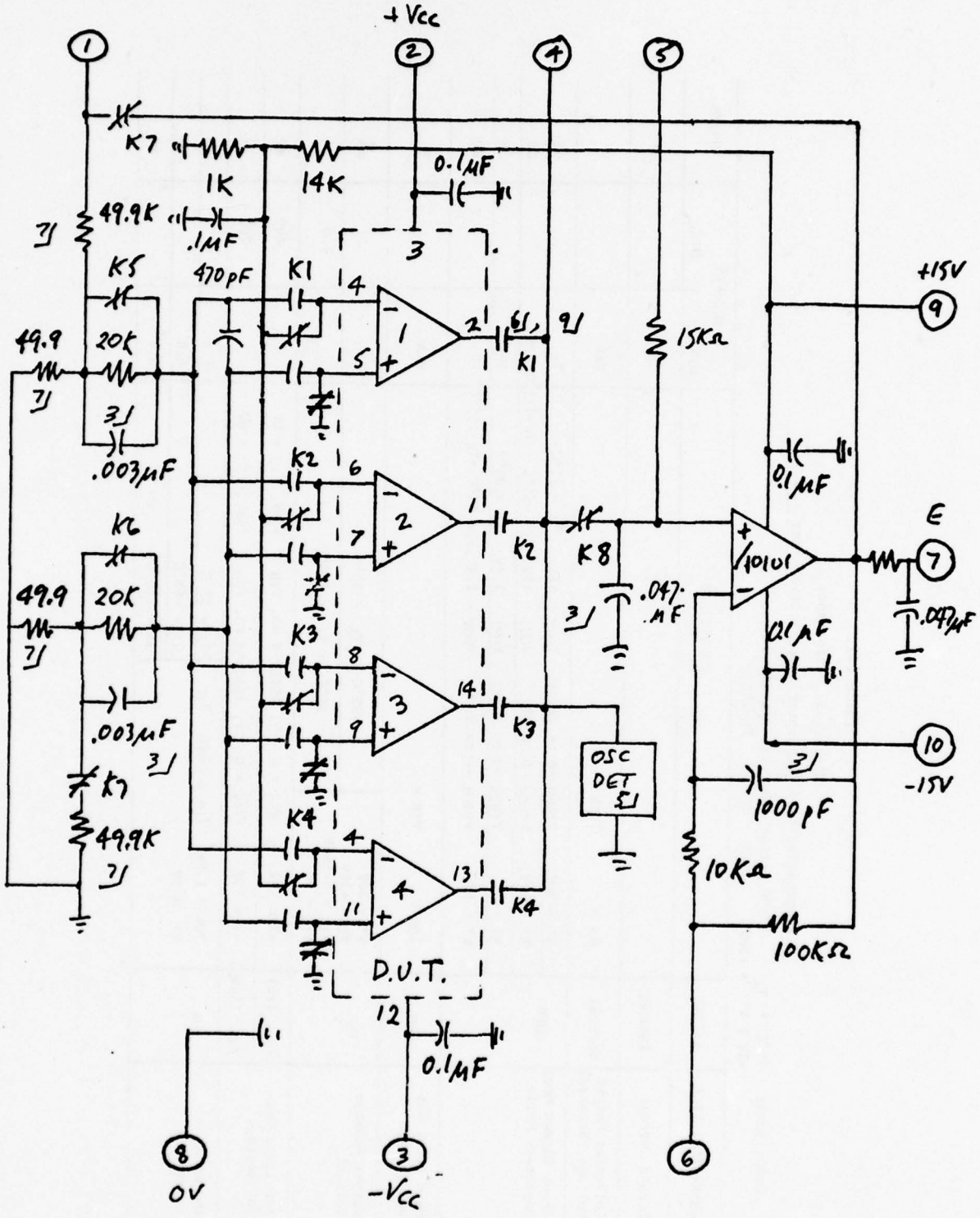
Table 4-1.

Electrical Performance

Proposed Voltage Comparator Specifications for 139

CONDITIONS: $-55°C < T_A < +125°C$ unless otherwise specified
$+5V \leq V^+ \leq +30V$ $-V=0V$ $R_L=15K$ $R_S=10K$

CHARACTERISTICS	SYMBOL	CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Strobe Current	I_{STROBE}			N/A		mA
Collector Output Voltage (Strobed)	$V_{O(STB)}$	Rs = I_{STB} =		N/A		V
Input Common Mode Rejection Ratio	CMRR	V^+ = 30V, V_{INCM} =0 to 28.5V, V_{OUT} = 15V, T_A = 25°C		76		dB
		V^+ = 30V, V_{INCM} =0 to 28V, V_{OUT} = 15V, T_A= -55°C + T_A=125°C		76		dB
		V^+ = 5V, V_{INCM} =0 to 3.5V, V_{OUT} = 1.4V T_A + 25°C		70		dB
		V^+ = 5V, V_{INCM} =0 to 3.0V, V_{OUT} = 1.4V, T_A+-55°C +T_A=125°C		70		dB
High Level Output Voltage	V_{OH}	I_{OH} = V_{ID} =		N/A		V
Output Leakage Current	I_O	V^+ = 30V, V_O = +30V, V_{ID} = <-15mV, V_{IC} = 0V	-55°C < T_A < 25°C		.1	µA
			25°C < T_A < 125°C		1.0	µA
Low Level Output Voltage	V_{OL1} (25)	+Vcc =5V V, -Vcc = 0 V, I_{SINK}=4 mA, $V_{ID} \geq$ 15mV, V_{IC} = 0V			400	mV
	V_{OL2} (temp)	+Vcc =5V V, -Vcc = 0 V, I_{SINK}=4 mA, $V_{ID} \geq$ 15mV, V_{IC} = 0V			700	mV
Output Sink Current	I_{OL}	V_{OL} = 1.5V, $V_{ID} \geq$ 15mV V_{IC}, V^+ = 5V	T_A = 25°C	8.0		mA
			T_A = -55°C	6.0		mA
			T_A = 125°C	6.0		mA



See following table and notes

Figure 4-1. Test circuit for static and dynamic tests

NOTES:

1. Test circuit pin conditions shall be as specified in the schedule of this figure.

2. Subgroups, test temperatures and limits shall be as specified in Table III of the slash sheet.

3. As required to prevent oscillations. Also, proper wiring procedures shall be followed to prevent oscillations. Loop response and settling time shall be consistant with test rate such that any value has settled to within 5% of its final value before measuring. Suggested values shown may not ensure loop stability for all layouts. Actual compensation also shall be approved by preparing activity prior to use.

4. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket.

5. Any oscillation greater than 300 mV (pk-pk) shall be cause for device failure.

6. Relays K1-K4 select the comparator under test. Idle comparators have 1V applied to the (-) input to force their outputs to the low state.

7. These resistors are ± 0.1% tolerance matched to ± .01%. All other resistors are ± 1% tolerance and capacitors are 10% tolerance.

8. Common mode rejection is calculated using the offset voltage values measured at the common mode range end points.

9. The relays shown indicate test connections only. All relays are shown in their de-energized states. Relay coils are not shown.

10. To minimize thermal drift, the reference voltage for gain measurement E_3 shall be taken immediately prior to or after reading E_{22} and E_{23}.

11. Saturation of the nulling amplifier is not allowed on tests where E value is measured.

12. The equations take into account both the closed loop gain of 1000 and the scale factor multipliers, so that the calculated values are in comparable units as listed in Tables 1 and 3 of the slash sheet.

Figure 4-1. Test circuit for static and dynamic tests (cont'd)

Parameter Symbol	Programmable Adapter Pins [1] 1	2	3	4	5	6	Relays Energized	Pin Measured No	Value	Unit	Equation	Unit
V_{IO}	-	30V	0V	-	30V	15V	-	7	E_1	V	$V_{10} = E_1$	mV
	-	2V	-28V	-	2V	-15V			E_2		$V_{10} = E_2$	
	-	15V	-15V	-	15V	0V			E_3		$V_{10} = E_3$	
	-	5V	0V	-	5V	1.4V			E_4		$V_{10} = E_4$	
I_{10}	-	30V	0V	-	30V	15V	K5, K6	7	E_5	V	$I_{10} = 50\ (E_1-E_5)$ [12]	nA
	-	2V	-28V	-	2V	-15V			E_6		$I_{10} = 50\ (E_2-E_6)$	
	-	15V	-15V	-	15V	0V			E_7		$I_{10} = 50\ (E_3-E_7)$	
	-	5V	0V	-	5V	1.4V			E_8		$I_{10} = 50\ (E_4-E_8)$	
$+I_{1B}$	-	30V	0	-	30V	15V	K6	7	E_9	V	$+I_{1B} = 50\ (E_1-E_9)$	nA
	-	2V	-28V	-	2V	-15V			E_{10}		$+I_{1B} = 50\ (E_2-E_{10})$	
	-	15V	-15V	-	15V	0V			E_{11}		$+I_{1B} = 50\ (E_3-E_{11})$	
	-	5V	0V	-	5V	1.4V			E_{12}		$+I_{1B} = 50\ (E_4-E_{12})$	
$-I_{1B}$	-	30V	0	-	30V	15V	K7	7	E_{13}	V	$-I_{1B} = 50\ (E_{13}-E_1)$	nA
	-	2V	-28V	-	2V	-15V			E_{14}		$-I_{1B} = 50\ (E_{14}-E_2)$	
	-	15V	-15V	-	15V	0V			E_{15}		$-I_{1B} = 50\ (E_{15}-E_3)$	
	-	5V	0V	-	5V	1.4V			E_{16}		$-I_{1B} = 50\ (E_{16}-E_4)$	
$\triangle V_{10}/\triangle T$	Calculate $(E_1 @ T - E_1 @ 25°C)\ 10^3 / \lvert 25°C - T \rvert$											uV/°C
$\triangle I_{10}/\triangle T$	Calculate $((E_1-E_5) @ T - (E_1-E_5) @ 25°C)\ 10^4 / \lvert 25°C - T \rvert$											pA/°C
CMR	Calculate $20 \log (30000 / E_1-E_2)$ [8]											dB
I_{CEX}	-15V	30V	0V	30V	0V	0V	K7, K8	4	I_{17}	nA	$I_{CEX} = I_{17}$	nA
V_{OL}	15V	4.5V	0V	4mA	0V	0V	K7, K8	4	E_{18}	V	$V_{OL} = E_{18}$	V
	15V	4.5V	0V	6mA	0V	0V			E_{19}		$V_{OL} = E_{19}$	
I_{cc}	-15V	5V	0V	-	0V	0V	K7, K8	2	I_{20}	mA	$I_{cc} = I_{20}$	mA
	-15V	30V	0V	-	0V	0V			I_{21}		$I_{cc} = I_{21}$	
+ AV	-	15V	-15V	-	15V	10V	-	7	E_{22}	V	$+AV = \frac{10}{E_3-E_{22}}$, $-AV = \frac{10}{E_{23}-E_3}$	V/mV
- AV	-	15V	-15V	-	15V	-10V	-	7	E_{23}	V		

Table 4-2. Test conditions for use with figure 4-1 test circuit.

SECTION V

MIL-M-38510/101E
SINGLE AND DUAL OPERATIONAL AMPLIFIERS

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SECTION V

MIL-M-38510/101E

SINGLE AND DUAL OPERATIONAL AMPLIFIERS

5.1 Background and Introduction

The op amp specification /101 is one of the more mature military linear documents. Even though it was at revision D when the contract effort began, a number of problems existed with it. GEOS effort aimed at resolving the problems so that IC vendors could more readily test and accept devices conforming to the specification without sacrificing reliability. The following device types are covered by this specification:

Device Type	Commercial Type
01	741A
02	747A
03	LM101A
04	LM108A
05	LH2101A
06	LH2108A
07	LM118

Although seven device types are cited, only four distinct sets of electrical specifications exist because some types are the "duals of others". Device types 02, 05 and 06 are the duals of 01, 03 and 04 respectively. As of May 12, 1977, the following manufacturers were on the QPL (Qualified Products List).

Manufacturer	01	02	03	04	05	06	07
AMD	PI	PII	PI	PII			
Fairchild	PI	PI	PI	PI			
National	PI	PII	PI	PI			PII
Intersil	PI						
Raytheon	PI						
Signetics							
Motorola							
RCA							
T.I.							
Harris							

Note: PI - Fully qualified
PII - Conditionally qualified
PII qualification is dropped 30 days after any vendor achieves PI qualification.

Figure 5-1. QPL sources of device types

It is seen that, of the potential vendors, not many are qualified to make /101 devices. A telephone survey was made, initially, of all vendors to list their /101 problems. The vendor problems were studied and entered into matrix charts. Not all of the problems were valid, since some seemed to be misinterpretations of the specifications. A joint industry organization, the JC-41 Committee on Linear IC's, was also solicited for technical inputs to improve the /101 specifications.

5.2 Description of Device Types

5.2.1 Common Device Characteristics

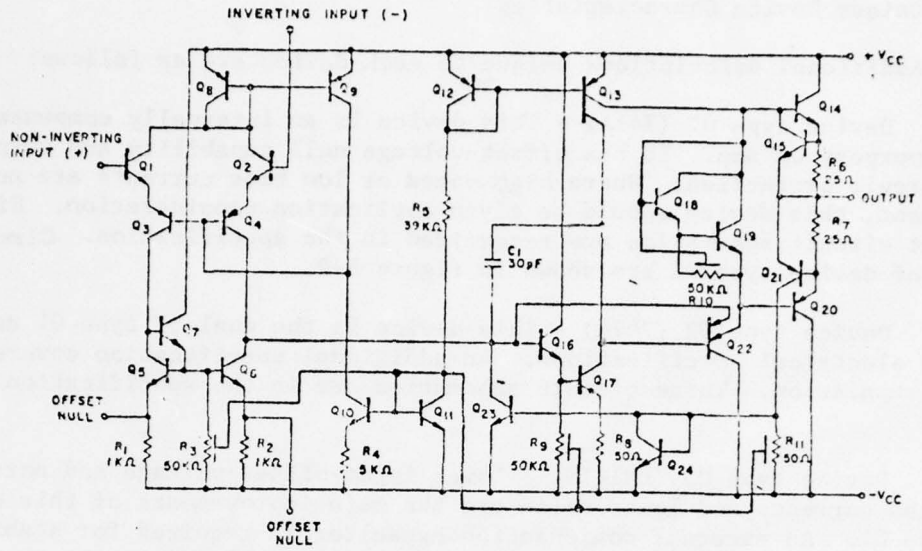
Each of the following operational amplifiers have a number of common characteristics. They all have a differential input stage in order to provide high gain for differential signals and much lower gain for signals common to both inputs. The two inputs are called the inverting (-) and non-inverting (+) inputs. For each unique design different techniques are used to enhance the desired input characteristics. Low input-offset voltage, low bias current, high gain, high input impedance and high common-mode rejection are the main desired input characteristics. Next, a level-shifting intermediate stage exists to provide further signal amplification. This stage can be differential or single-ended with a variety of interconnections to the output stage.

The output stage almost always takes the form of a complementary emitter follower to provide a single-ended, low-impedance output signal. This stage is generally biased class A-B so that the conductive ranges of the sinking and sourcing transistors overlap. Otherwise a deadband would exist in the output signal. The resulting signal distortion, although reduced by the loop gain of the entire op amp in its application, may still be objectionable. Sometimes the output stage is biased class B, if low power dissipation is an important parameter. In /101 all of the devices have class A-B outputs.

All outputs have current-limit circuits to protect the amplifier from output shorts to ground or to either supply rail. The mechanization involves a transistor whose base-emitter junction is in parallel with an output resistor and whose collector goes to the base of the output-sourcing transistor. For the output-sinking transistor, the method is similar, except that the collector of the current-limiting transistor goes to an intermediate point. In either case, however, base drive to the output transistor is shunted away as the voltage drop across the current-limit resistor approaches V_{BE}.

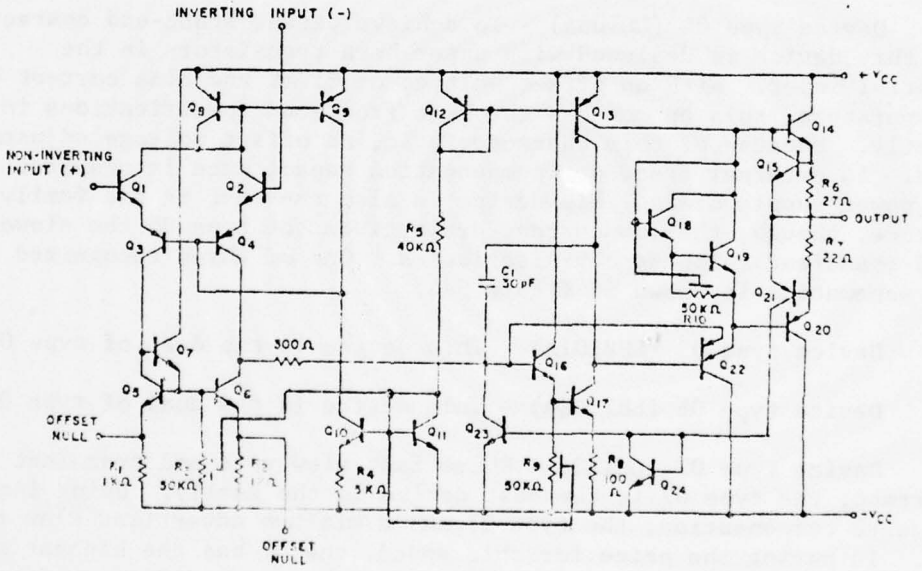
All op amps require frequency compensation to be built internally or taken care of externally. Without frequency compensation, any normal feedback application of the op amp would result in oscillations. This occurs when the sum of the phase shifts introduced by each gain stage exceeds 180^{o} before the loop gain is "rolled-off" to less than 0 dB.

Device type 01, Circuit A



NOTE: All resistance and capacitance values are nominal.

Device type 01, Circuit B



NOTE: All resistance and capacitance values are nominal.

Figure 5-2. Device type 01 circuits

5.2.2 Unique Device Characteristics

Additional descriptions unique to each device are as follows:

5.2.2.1 Device type 01 (741A) - This device is an internally compensated, general purpose op amp. It has offset-voltage null capability and output short-circuit protection. Where high speed or low bias currents are not a requirement, this device should be given application consideration. Eight different circuit schematics are recognized in the specification. Circuits A and B of device type 01 are shown in figure 5-2.

5.2.2.2 Device type 02 (747A) - This device is the dual of type 01 and has the same electrical specifications. An additional specification covers channel separation. Three circuit schematics are in the specification for type 02.

5.2.2.3 Device type 03 (LM101N) - Lower input-offset voltage and current, lower bias currents and lower noise are the main improvements of this device over type 01. An external compensation capacitor is required for stability and bandwidth trade-offs. In order to achieve lower bias currents then type 01, the input stage is configured with latest PNP transistors Q_3 and Q_4 biased through a common current source. This can be seen in circuit C of type 03 shown in figure 5-3.

5.2.2.4 Device type 04 (LM108A) - To achieve better front-end characteristics, this device is designed with super-beta transistors in the differential input. With an offset voltage of ±1 mV and bias current of 3 nA over temperature, this op amp has the best front-end specifications in the /101 family. Because of this characteristic, no offset voltage adjustment is provided. An external frequency compensation capacitance is required. For minimum power supply drain, this device is also the best in the family. As a consequence, though, the low current drain gives the type 04 the slowest slew rate and transient response characteristics. One of three recognized type 04 circuit schematics is shown in figure 5-4.

5.2.2.5 Device type 05 (LH2101A) - This device is the dual of type 03.

5.2.2.6 Device type 06 (LH2108A) - This device is the dual of type 04.

5.2.2.7 Device type 07 (LM118) - Where fast slew rate and transient response is important, the type 07 is the best device in the family. Using internal feed-forward compensation, the type 07 has a minimum advertised slew rate of 50 V/us. In paying the price for this speed, the 07 has the highest supply current, offset voltage and bias currents of any in the /101 specification. A circuit schematic of type 07 is shown in figure 5-5.

5.3 Tabulation of Parameter Limit Changes

The following four tables list the parameters, test conditions and limit values of the device types in the /101 specification. Four columns of limits are shown, beginning with the intitial /101D values and ending with a

GEOS recommendation for /101E. The rough draft /101E specification submitted to RADC has the same limits as these GEOS recommendations. The middle two columns give the originating vendor's catalog values and the recommended values of the JC-41 Committee.

5.4 Discussion

5 4.1 Specification Change Guidelines

In making the recommendations for the /101E specification, the following guidelines were used.

5.4.1.1 /101D and its amendments were examined to ferret out mistakes and inconsistencies.

5.4.1 2 The loosening of limits was made with reluctance and then only when the vendors presented a strong and valid reason for them.

5 4.1.3 With any proposed specification "loosening" the interests of the user must be protected so that after the fact he is not forced to add special acceptance tests for the device to work in his circuits. This guideline cannot be guaranteed for user applications which are "shaky" to begin with.

5.4.1.4 The changes made, if in an "opening" direction, should have a high reward-to-risk ratio so that the benefits of increased yield and lower future cost do not result in reliability degradation.

5.4.1.5 There were many recommendations to loosen the -01 (741) specifications, but because of possible user problems, this was resisted. Next a second-tier 741 specification was proposed. This would have added a new device (-08) with specifications inferior to the -01. A dubious precedent would have been established. None of the vendors furnished device data to substantiate their requests for specification changes.

5.4.2 Reason for Specific Changes

The reasons for most specification changes are shown in the notes section of the parameter tabulations. Further discussion of the more significant changes follows:

5.4.2.1 I_{10} Delta - This sample test was deleted because it represents a change of a change and, as such, demands unwarranted time-drift stability of the test equipment.

5.4.2.2 $I_{OS(+)}$, $I_{OS(-)}$ - For throughput considerations, short circuit current is measured automatically as are all other 100% d-c tests. Since only milliseconds of time are needed to make the test, device self-heating is minimal and the measured current is therefore greater than the steady state

value. Consequently, the limits were raised. The test adequately checks this protective feature with a specified test time of t $\leq$ 25 milliseconds.

5.4.2.3 V_{IO} ADJ (+), V_{IO} ADJ (-) - These tests were corrected and modified to insure that the adjustment range is one millivolt greater in the correct direction than the worst case offset voltage limits.

5.4.2.4 I_{CC} - For power supply sizing purposes, this parameter is much more useful than power dissipation. By specifying I_{CC} at ±15 V instead of ±20 V, the user can conservatively determine current drain at either voltage (i.e. I_{CC} at 20 V = 20/15 I_{CC} at 15 V). It would be risky to go the other way.

5.4.2.5 V_{OP} - Loaded voltage swing is measured from ground to the plus and minus output swing limits. Therefore, it makes more sense to specify it in this manner than to specify the sum as has been done in the past. Also a small swing in one direction cannot be compensated for by a large swing in the other direction.

5.4.2.6 TR (t_r), TR (OS) - These transient response limits have given the vendors the most problems. Some vendors have alleged that the rise time and overshoot limits were initially established by taking the best numbers from mixed lots of devices (i.e., fast rise times with low overshoots).

In order to provide relief, the overshoot limits were relaxed across the board. The other alternative which JC-41 recommended was to leave the limits alone, but add 100 pF of capacitance across the feedback resistor of the test circuit. From transient response test observations at GEOS, this much capacitance masks the characteristics of the device under test. Instead GEOS recommends a maximum of 10 pF, including strays, while allowing wider overshoot limits than before.

5.4.2.7 SR (+), SR (-) - With device type 07 in /101D a "lop-sided" slew rate existed with SR (+) = 75 V/us (minimum) and SR (-) = 50 V/us (minimum). This reflected the characteristics of vendor C's device. Since a user cannot generally take advantage of this peculiarity and since different vendor devices had different characteristics, it was recommended that symmetrical limits of ±50 V/us (minimum) be established after vendors B and C had agreed to a ±50 V/us spec. A third one, vendor A, had yield problems and would have preferred a ±40 V/us spec. Since, in the case of type 07, slew rate is one of the most important parameters, GEOS recommends a firm stand on the ±50 V/us slew rate limits.

5.4.2.8 ts (+), ts (-) - Settling time was changed from a sampled test to a qualification test for several reasons.

1) It is design dependent rather than lot dependent.

2) Its value can be inferred from rise time and overshoot data.

5.4.2.9 N1 (BB), Ni (PC) - The JC-41 Committee recommended a new test circuit to measure broadband and popcorn noise. This method was reviewed and approved by GEOS. With this new method, nulling amplifier noise does not contribute to the noise of the device under test. As in /101D, the test time required to measure popcorn noise is 15 seconds.

5.4.3 /101 Document Corrections

The following change recommendations are offered to correct minor discrepancies in the /101 document.

5.4.3.1 In table III, tests should be added for V_{IO}, I_{IO}, $+I_{IB}$ and $-I_{IB}$ for the conditions $V_{CC} = \pm 5$ V, $V_{CM} = 0$ at $T_A = -55^{o}C$ and $T_A = 125^{o}C$. Table I does not exclude these conditions.

5.4.3.2 The symbol V_{opp} should be replaced with V_{op} wherever it appears to reflect zero-to-peak swing measurements.

5.4.3.3 The noise test circuit shown in /101, figure 10, could be eliminated by incorporating the same information in figure 8 and its associated table, (i.e., additional switches could accomplish this).

5.4.3.4 The /101 figure 8 test circuit and its associated table is very important for defining all test conditions. It would be easier to follow if the switches were replaced with relay contacts and if their configuration in the table were defined in terms of 1's and 0's to show their respective states. This is being done in the /110 quad op amp spec. A copy of its associated test circuit and table is attached in the quad op amp section of this report.

5.4.3.5 In Amendment 2 of /101D the schematic on page 17 is labeled "Device type 04 and 05, Circuit B". The "05" should be replaced with "06".

5.4.3.6 In figure 8, switch S6 shows an open for the condition to force the device under test (DUT) to zero at the output. It is bad practice to leave an op amp input "open" for noise considerations. A better solution is to eliminate S6 and define the desired voltage in the table.

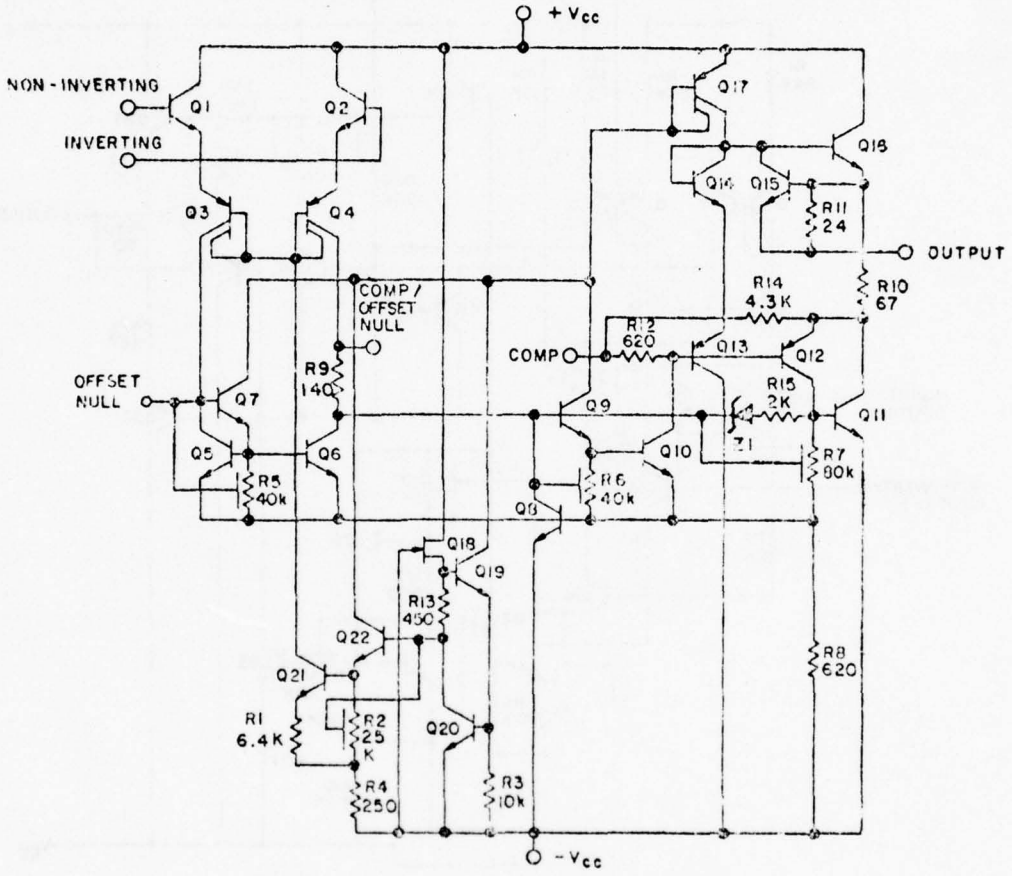
5.5 Conclusion

The effort expended in modifying MIL-M-38510/101 was to make the document more usable to vendors and users alike. It was not a characterization effort in which devices were measured and analyzed. No raw data from any vendors was seen. Many of the changes were made to improve vendor throughputs and yield without affecting the basic reliability of the devices. Much of the work on this program is not readily visible or covered in this report. Consulting with vendors on problems and solutions did not necessarily result in changes to the /101 documents. The technical content of all such conversations has been entered in a log book. Trip reports and monthly progress reports also document related efforts.

5.6 Recommendations for Future Efforts

An important parameter which may require future effort is that of voltage gain, Avs. Many op amps have much higher gain than the commonly specified value of 25 V/mV over temperature. With these high open-loop gains, measured under load, thermal effects distort the measurement. Even the polarity of the gain measurement can be changed by the thermal effects. At present the specification does not define or exclude the thermal effects from the true open-loop gain. Since these effects are real, the specification should deal with them. Otherwise, the screening value of the parameter is lost. The effect of the thermal influence also changes with time. Pending any further analysis, it is recommended that the gain be measured at a high enough load resistance to minimize thermal effects.

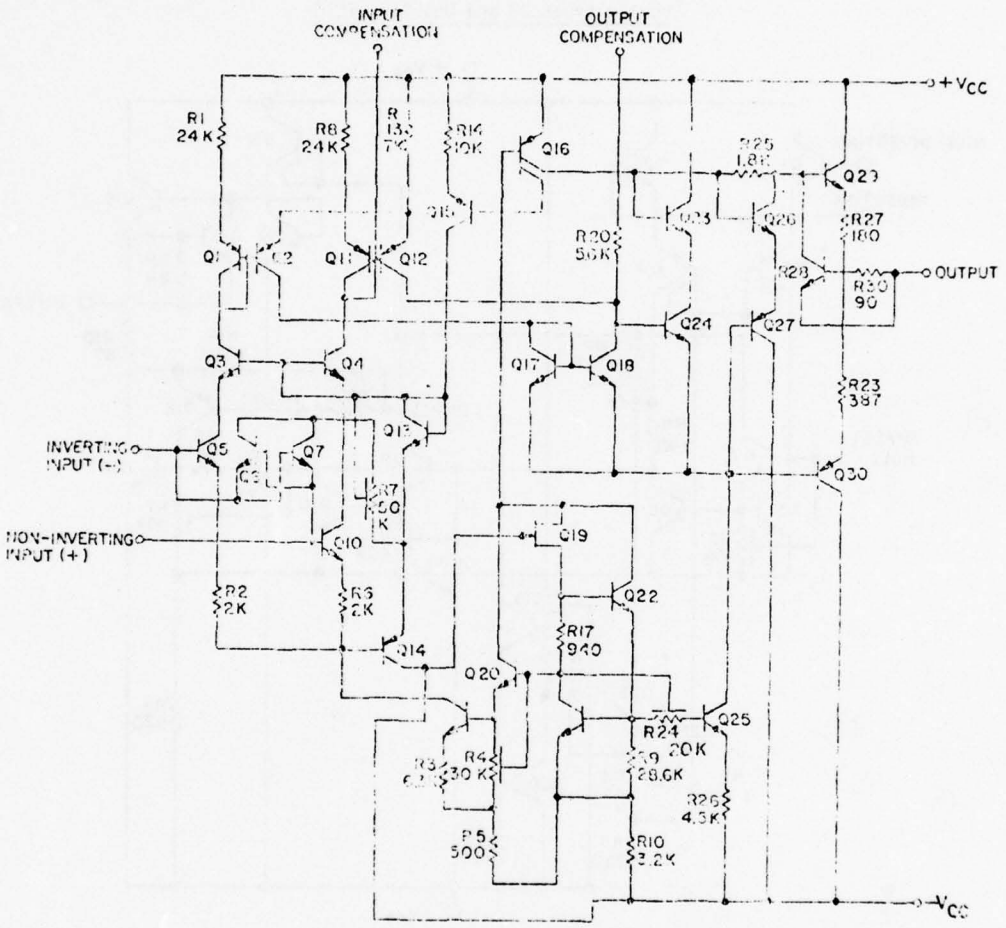
Device types 03 and 05, Circuit C



NOTES:
1. All resistance and capacitance values are nominal.
2. For device type 05, the circuit shown is for each amplifier.

Figure 5-3. Device type 03 and 05, circuit C

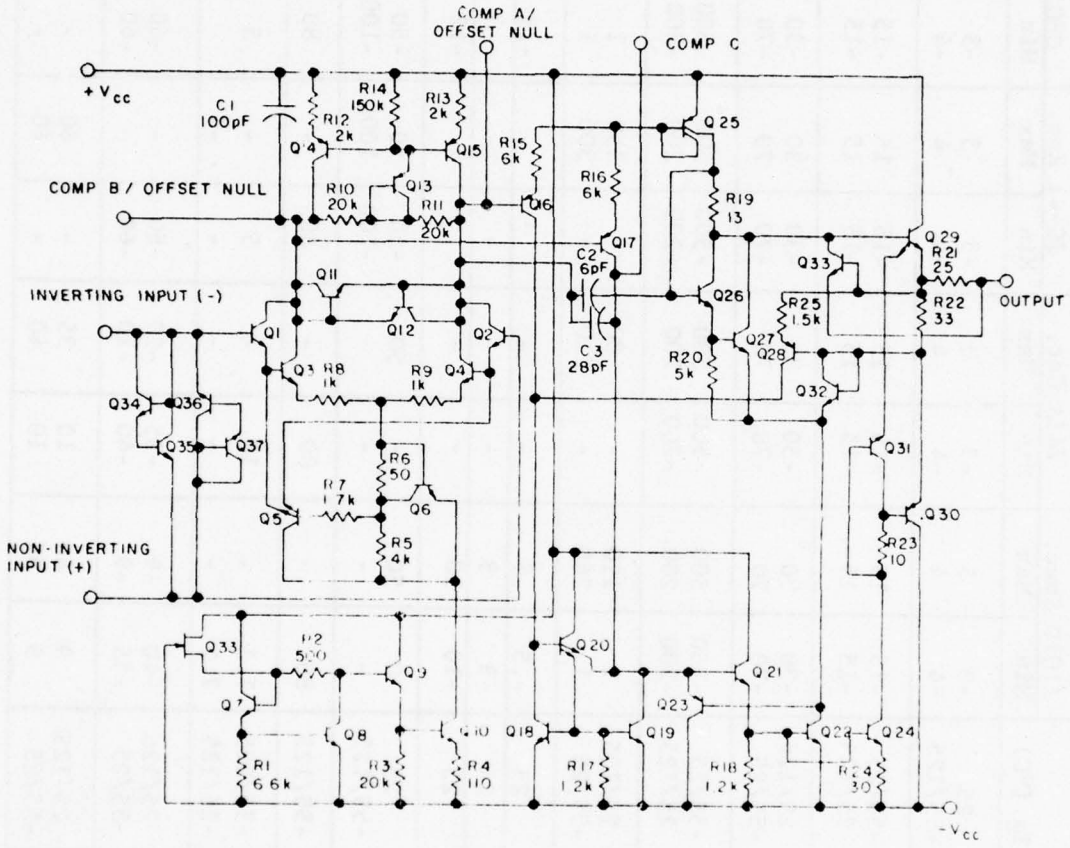
Device types 04 and 06, Circuit A



NOTES:
1. All resistance and capacitance values are nominal.
2. For device type 05, the circuit shown is for each amplifier.

Figure 5-4. Device type 04 and 06, circuit A

Device type 07



NOTE: All resistance and capacitance values are nominal.

Figure 5-5. Device type 07

Table 5-1. Operational amplifier M38510/10101, /10102 (741A, 747A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	741A Cat. Min	741A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS /101E Min	GEOS /101E Max	Units
	V_{IO}	2/	25 -55/125	-3 -4	3 4	-3 -4	3 4	-3 -4	3 4	-3 -4	3 4	mV
	$\frac{\Delta V_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25 25/125	-15 -15	15 15	-15 -15	15 15	-15 -15	15 15	-15 -15	15 15	uV/°C
	I_{IO}	2/	25/125 -55/25	-30 -70	30 70	-30 -70	30 70	-30 -70	30 70	-30 -70	30 70	nA
	$\frac{\Delta I_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25 25/125	-500 -200	500 200	-500 -200	500 200	-500 -200	500 200	-500 -200	500 200	pA/°C
	$+I_{IB}, -I_{IB}$	2/	25/125 -55/25	1 1	110 265	- -	80 210	- -	150 300	1 1	110 265	nA
	V_{IO} Delta	3/	25	-.5	.5	-	-			-.5	.5	mA
*	I_{IO} Delta	4/	25	-3	3	-	-	-	-	-	-	nA
*	I_{IB} Delta		25	-10	10	-	-			-12	12	nA
	+PSRR,	5/, 6/	25	0	50	-	50	-50	50	-50	50	uV/V
*	-PSRR		-55/125	-	-	-	-	-100	100	-100	100	
	CMR	6/	-55/125	80	-	80	-	80	-	80	-	dB
*	V_{IO} ADJ(+)	6/	-55/125	7.5	-	10	-	5	-	5	-	mV
	V_{IO} ADJ(-)		-55/125	7.5	-	-	-	-	-5	-	-5	
*	I_{OS} (+)	$\pm V_{CC}$=15 V, 7/ t ≤ 25 ms	25/125 -55/25	-40 -55	-9 -9	-35 -40	-10 -10	-60 -60	- -	-60 -60	- -	mA
*	I_{OS} (-)	$\pm V_{CC}$ =15 V, 7/ t ≤ 25 ms	25/125 -55/25	9 9	40 55	10 10	35 40	- -	60 60	- -	60 60	mA

Table 5-1 (cont'd) Operational amplifier M38510/10101, /10102 (741A, 747A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec Min	/101D Spec Max	741A Cat. Min	741A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS, /101E Min	GEOS, /101E Max	Units
*	P_D	8/	-55	10	165	-	165	8/		8/		mW
			25	10	150	-	150					
			125	10	135	-	135					
*	I_{CC}	$\pm V_{CC}$=±15 V	-55	-	-	-	3.3	-	4.2	-	4.2	mA
		8/	25	-	-	-	2.8	-	3.8	-	3.8	
			125	-	-	-	2.5	-	3.4	-	3.4	
*	Z_{1S1}, Z_{1S2}		25	1	-	1	-	9/		9/		MΩ
			-55/125	0.5	-	0.5	-					
*	V_{op}	R_L=10 KΩ	-55/125	32	-	±16	-	±16	-	±16	-	V
		R_L=2 KΩ		30	-	±15	-	±15	-	±15	-	
	AVS (±)	R_L = 2 KΩ,	25	50	-	50	-	50	-	50	-	V/mV
*		10 KΩ	-55/125	32	-	32	-	25	-	25	-	
	AVS 10/	$\pm V_{CC}$ = ±5 V, R_L = 2 KΩ	-55/125	10	-	10	-	10	-	10	-	V/mV
	TR (tr)	11/ V_{IN}=50mV	-55/125	-	800	-	800	-	800	-	800	ns
*	TR (OS)		-55/125	-	20	-	20	-	20	-	25	%
*	BW	12/	-55/125	.43	-	.437	-			12/		MHz
*	SR(+),SR(-)	13/ V_{IN}=-5→	25/125	.3	-	.3	-	.3	-	.3	-	V/us
		+5 V Step	-55	.3	-	.3	-	.3	-	.3	-	
	ts(+),ts(-)	14/	25	-	-	-	-	-	-	-	-	ns
			-55/125	-	-	-	-	-	-	-	-	
	CS		25	80	-	100	-	80	-	80	-	dB

Table 5-1 (cont'd) Operational amplifier M38510/10101, /10102 (741A, 747A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	741A Cat. Min	741A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS, /101E Min	GEOS, /101E Max	Units
*	N1 (BB)	15/	25	-	15	-	-	-	15	-	15	uV rms
*	N1 (PC)		25	-	40	-	-	-	40	-	40	uV PK

NOTES:

1/ Unless otherwise specified, the supply voltages are $\pm V_{CC} = \pm 20$ VDC.

2/ This parameter is tested at $\pm V_{CC} = \pm 20$ V with $V_{CM} = 0$ V, -15 V and +15 V and also at $\pm V_{CC} = \pm 5$ V with $V_{CM} = 0$ V.

3/ These end point parameters are only measured following life and burn-in tests.

4/ I_{IO} Delta should be deleted because it represents a small change of a change and is difficult to measure, $\pm I_{IB}$ Delta should be sufficient.

5/ Amendment 1 corrected the 0 (Min) limit.

6/ In /101D, ±PSRR, CMR and V_{IO} ADJ were tested at 25°C only.

7/ JC-41 recommends that the short circuit be to ground instead of the opposite supply rail. GEOS recommends no change in the short to the rails, but a precautionary note should be added to indicate that I_{OS} protection cannot be guaranteed if T_A exceeds 75°C.

8/ It is recommended that P_D at $\pm V_{CC} = \pm 20$ V be replaced with I_{CC} at $\pm V_{CC} = \pm 15$ V because it is a more meaningful parameter for the design engineer.

9/ Parameters Z_{1S1} and Z_{1S2} should be deleted because they are not tested for in Table III and bias current limits over the common-mode range covers the DC input impedance (resistance).

10/ Test method change is recommended such that V_{IO} is not used in the AVS calculation.

Table 5-1 (cont'd). Operational amplifier M38510/10101, /10102 (741A, &47A)

NOTES:

11/ Originally C_F = 0 and many vendors had trouble with this spec. JC-41 wanted to make C_F = 100 pF. GEOS data indicates that with C_F = 100 pF, the device is masked. Instead GEOS recommends a limit change and C_F = 10 pF.

12/ GEOS recommends that this spec be deleted. It is calculated from 0.35/tr.

13/ JC-41 and GEOS recommend $\triangle$V points increased from ±1 V to ±2.5 V thus making the measurement more amendable to automatic test equipment.

14/ Settling time is not tested because normal user need of this parameter does not warrant the required bench test effort.

15/ A new test circuit exists in /101E. The new test eliminates nulling amplifier noise and is more accurate in distinguishing between broadband and popcorn noise.

* Changed limits on test conditions between /101D and /101E.

Table 5-2. Operational amplifier M38510/10103, /10105 (LM101A, LH2101A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM101A Cat. Min	LM101A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS, /101E Min	GEOS, /101E Max	Units
*	V_{IO}	2/	25	-1.5	1.5	-2	2	-2	2	-2	2	mV
			-55/125	-3	3	-3	3	-3	3	-3	3	
	$\frac{\Delta V_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25	-15	15	-15	15	-15	15	-15	15	uV/°C
			25/125	-15	15	-15	15	-15	15	-15	15	
	I_{IO}	2/	25/125	-10	10	-10	10	-10	10	-10	10	nA
			-55/25	-20	20	-20	20	-20	20	-20	20	
*	$\frac{\Delta I_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25	-150	150	-200	200	-200	200	-200	200	pA/°C
			25/125	-100	100	-100	100	-100	100	-100	100	
*	$+I_{IB}$, $-I_{IB}$	2/	25/125	1	65	-	75	1	75	1	75	nA
			-55/25	1	100	-	100	1	100	1	100	
*	V_{IO} Delta	3/	25	-.4	.4	-	-	-.5	.5	-.5	.5	mV
*	I_{IO} Delta	4/	25	-2	2	-	-	-	-	-	-	nA
*	I_{IB} Delta		25	-6.5	6.5	-	-	-7.5	7.5	-7.5	7.5	nA
*	+PSRR,	5/, 6/	25	0	50	-	-	-50	50	-50	50	uV/V
*	-PSRR		-55/125	-	-	(80	dB)	-100	100	-100	100	
*	CMR	6/	-55/125	90	-	80	-	80	-	80	-	dB
*	V_{IO} ADJ(+)	6/	-55/125	7.5	-	-	-	+4	-	+4	-	mV
*	V_{IO} ADJ(-)		-55/125	7.5	-	-	-	-	-4	-	-4	
*	I_{OS} (+)	$\pm V_{CC}$=15 V, 7/ t ≤ 25 ms	25/125	-40	-9	-	-	-60	-	-60	-	mA
			-55/25	-55	-9	-	-	-60	-	-60	-	
*	I_{OS} (-)	$\pm V_{CC}$=15 V, 7/ t ≤ 25 ms	25/125	9	40	-	-	-	60	-	60	mA
			-55/25	9	55	-	-	-	60	-	60	

Table 5-2 (cont'd). Operational amplifier M38510/10103, /10105 (LM101A, LH2101A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM101A Cat. Min	LM101A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS, /101E Min	GEOS, /101E Max	Units
*	P_D	8/	-55	10	140	-	-					mW
			25	10	120	-	-	8/		8/		
			125	10	100	-	-					
*	I_{CC}	$\pm V_{CC}$=±15 V	-55	-	-	-	-	-	3.5	-	3.5	mA
		8/	25	-	-	-	3.0	-	3.0	-	3.0	
			125	-	-	-	2.5	-	2.5	-	2.5	
*	Z_{1S1}, Z_{1S2}		25	1.5	-	1.5	-	9/		9/		MΩ
			-55/125	1	-	-	-					
*	V_{op}	R_L=10 KΩ	-55/125	32	-	±12	-	±16	-	±16	-	V
		R_L= 2 KΩ		30	-	±10	-	±15	-	±15	-	
*	AVS (±)	R_L = 2 KΩ,	25	100	-	50	-	50	-	50	-	V/mV
		10 KΩ	-55/125	50	-	25	-	25	-	25	-	
	AVS 10/	$\pm V_{CC}$ =±5 V, R_L = 2 KΩ	-55/125	10	-	-	-	10	-	10	-	V/mV
	TR (tr)	V_{IN}-50 mV 11/	-55/125	-	800	-	-	-	800	-	800	ns
*	TR (OS)		-55/125	-	20	-	-	-	25	-	25	%
	BW	12/	-55/125	.43	-	-	-			12/		MHz
*	SR(+),SR(-)	13/V_{IN}=-5→	25/125	.3	-	-	-	.3	-	.3	-	V/us
		+5 V Step	-55	.2	-	-	-	.2	-	.2	-	
	ts(+),ts(-)	14/	25	-	-	-	-	-	-	-	-	ns
			-55/125	-	-	-	-	-	-	-	-	
	CS		25	80	-	-	-	80	-	80	-	dB

Table 5-2 (cont'd). Operational amplifier M38510/10103, /10105 (LM101A, LH2101A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM101A Cat. Min	LM101A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS /101E Min	GEOS /101E Max	Units
*	N1 (BB)	15/	25	-	10	-	-	-	15	-	15	uV rms
*	N1 (PC)		25	-	30	-	-	-	80	-	80	uV PK

NOTE:

1/ Unless otherwise specified, the supply voltages are $+V_{CC} = \pm 20$ VDC.

2/ This parameter is tested at $\pm V_{CC} = \pm 20$ V with $V_{CM} = 0$ V, -15 V and +15 V and also at $\pm V_{CC} = \pm 5$ V with $V_{CM} = 0$ V.

3/ These end point parameters are only measured following life and burn-in tests.

4/ I_{IO} Delta should be deleted because it represents a small change of a change and is difficult to measure, $\pm I_{IB}$ Delta should be sufficient.

5/ Amendment 1 corrected the 0 (Min) limit.

6/ In /101D, ±PSRR, CMR and V_{IO} ADJ were tested at 25°C only.

7/ JC-41 recommends that the short circuit be to ground instead of the opposite supply rail. GEOS recommends no change in the short to the rails, but a precautionary note should be added to indicate that I_{OS} protection at $T_A > 75°C$ cannot be guaranteed.

8/ It is recommended that P_D at $\pm V_{CC} = \pm 20$ V be replaced with I_{CC} at $\pm V_{CC} = \pm 15$ V.

9/ Parameters Z_{IS1} and Z_{IS2} should be deleted because they are not tested for in Table III and bias current limits over the common-mode range covers the DC input impedance (resistance).

10/ Test method change is recommended such that V_{IO} is not used in the AVS calculation.

Table 5-2 (cont'd). Operational amplifier M38510/10103, /10105 (LM101A, LH2101A)

NOTES:

11/ Originally C_F = 0 and many vendors had trouble with this spec. JC-41 wanted to make C_F = 100 pF. GEOS data indicates that with C_F = 100 pF the device is masked. Instead GEOS recommends a limit change and C_F = 10 pF.

12/ GEOS recommends that this spec be deleted. It is calculated from 0.35/tr.

13/ JC-41 and GEOS recommend $\triangle$V points increased from ±1 V to ± 2.5 V.

14/ Not tested.

15/ New test circuit in /101E.

* Changed limits on test conditions between /101D and /101E.

Table 5-3. Operational amplifier M38510/10104, /10106 (LM108A, LH2108A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM108A Cat. Min	LM108A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS, /101E Min	GEOS, /101E Max	Units
	V_{IO}	2/	25	-.5	.5	-.5	.5	-.5	.5	-.5	.5	mV
			-55/125	-1	1	-1	1	-1	1	-1	1	
	$\frac{\Delta V_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25	-5	5	-5	5	-5	5	-5	5	uV/°C
			25/125	-5	5	-5	5	-5	5	-5	5	
	I_{IO}	2/	25/125	-.2	.2	-.2	.2	-.2	.2	-.2	.2	nA
			-55/25	-.4	.4	-.4	.2	-.4	.4	-.4	.4	
	$\frac{\Delta I_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25	-2.5	2.5	-2.5	2.5	-2.5	2.5	-2.5	2.5	pA/°C
			25/125	-2.4	2.4	-2.5	2.5	-2.5	2.5	-2.5	2.5	
	$+I_{IB}$, $-I_{IB}$	2/	25/125	-2	2	-2	2	-2	2	-2	2	nA
			-55/25	-.1	3	-	3	-.1	3	-.1	3	
	V_{IO} Delta	3/	25	-.25	.25	-	-	-.25	.25	-.25	.25	mA
*	I_{IO} Delta	4/	25	-.1	.1	-	-	-	-	-	-	nA
*	I_{IB} Delta		25	-.2	.2	-	-	-.5	.5	-.5	.5	nA
*	+PSRR, -PSRR	5/, 6/	25	0	16	-	-	-16	16	-16	16	uV/V
			-55/125	-	-	(96	dB)	-16	16	-16	16	
	CMR	6/	-55/125	96	-	96	-	96	-	96	-	dB
	V_{IO} ADJ (+)	6/	-55/125	N/A	-	-	-	-	-	N/A	-	mV
	V_{IO} ADJ (-)		-55/125	N/A	-	-	-	-	-	N/A	-	
*	I_{OS} (+)	$\pm V_{CC}$=15 V, 7/ t ≤ 25 ms	25/125	-15	-2	-	-	-15	-	-15	-	mA
			-55/25	-15	-4	-	-	-15	-	-15	-	
*	I_{OS} (-)	$\pm V_{CC}$=15 V, 7/ t ≤ 25 ms	25/125	2	15	-	-	-	15	-	15	mA
			-55/25	4	15	-	-	-	15	-	15	

Table 5-3 (cont'd). Operational amplifier M38510/10104, /10106 (LM108A, LH2108A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM108A Cat. Min	LM108A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS, /101E Min	GEOS, /101E Max	Units
*	P_D	8/	-55	2	32	-	-	8/		8/		mW
			25	2	24	-	24					
			125	2	16	-	16					
*	I_{CC}	$\pm V_{CC}=\pm 15V$ 8/	-55	-	-	-	-	-	.8	-	.8	mA
			25	-	-	-	.6	-	.6	-	.6	
			125	-	-	-	.4	-	.6	-	.6	
*	Z_{1S1}, Z_{1S2}		25	20	-	30	-	9/		9/		MΩ
			-55/125	10	-	-	-					
*	Vop	R_L=10 KΩ	-55/125	32	-	(±13@V_{CC}=±15)		±16	-	±16	-	V
		R_L= 2 KΩ		N/A	-	-	-	N/A	-	N/A	-	
	AVS (±)	R_L = 2 KΩ, 10 KΩ	25	80	-	80	-	80	-	80	-	V/mV
			-55/125	40	-	40	-	40	-	40	-	
	AVS 10/	$\pm V_{CC}$ = ±5 V, R_L = 2 KΩ	-55/125	20	-	-	-	20	-	20	-	V/mV
*	TR (tr)	V_{IN}=50mV 11/	-55/125	-	1000	-	-	-	1000	-	1000	ns
	TR (OS)		-55/125	-	40	-	-	-	40*	-	50	%
*	BW	12/	-55/125	.35	-	-	-	-	-	12/		MHz
**	SR(+),SR(-)	V_{IN}=-5→+5 V Step 13/	25/125	.1	-	-	-	.05	-	.05	-	V/us
			-55	.08	-	-	-	.05	-	.05	-	
	ts(+),ts(-)	14/	25	-	-	-	-	-	-	-	-	ns
			-55/125	-	-	-	-	-	-	-	-	
	CS		25	80	-	-	-	80	-	80	-	dB

Table 5-3 (cont'd). Operational amplifier M38510/10104,/10106 (LM108A, LH2108A)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM108A Cat. Min	LM108A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS, /101E Min	GEOS, /101E Max	Units
*	N1 (BB)	15/	25	-	-	-	-	15	-	15	-	uV rms
*	N1 (PC)		25	-	-	-	-	40	-	40	-	uV PK

NOTES:

1/ Unless otherwise specified, the supply voltages are $\pm V_{CC} = \pm 20$ VDC.

2/ This parameter is tested at $\pm V_{CC} = \pm 20$ V with $V_{CM} = 0$ V, -15 V and +15 V and also at $\pm V_{CC} = \pm 5$ V with $V_{CM} = 0$ V.

3/ These end point parameters are only measured following life and burn-in tests.

4/ I_{IO} Delta should be deleted because it represents a small change of a change and is difficult to measure, $\pm I_{IB}$ Delta should be sufficient.

5/ Amendment 1 corrected the 0 (Min) limit.

6/ In /101D, ±PSRR, CMR and V_{IO} ADJ were tested at 25°C only.

7/ JC-41 recommends that the short circuit be to ground instead of the opposite supply rail. GEOS recommends no change in the short to the rails, but a precautionary note should be added to indicate that I_{OS} protection at $T_A > 75°C$ cannot be guaranteed.

8/ It is recommended that P_D at $\pm V_{CC} = \pm 20$ V be replaced with I_{CC} at $\pm V_{CC} = \pm 15$ V.

9/ Parameters Z_{1S1} and Z_{1S2} should be deleted because they are not tested for in Table III and bias current limits over the common-mode range covers the DC input impedance (resistance).

10/ Test method change is recommended such that V_{IO} is not used in the AVS calculation.

Table 5-3 (cont'd). Operational amplifier M38510/10104,/10106 (LM108A, LH2108A)

NOTES:

* 11/ Originally C_F = 0 and many vendors had trouble with this spec. JC-41 wanted to make C_F = 100 pF. GEOS data indicates that with C_F = 100 pF the device is masked. Instead GEOS recommends a limit change and C_F = 10 pF.

12/ GEOS recommends that this spec be deleted. It is calculated from 0.35/tr.

13/ JC-41 and GEOS recommend $\triangle$V points increased from ±1 V to ±2.5 V.

14/ Not tested.

15/ New test circuit in /101E.

* Changed limits on test conditions between /101D and /101E.

Table 5-4. Operational amplifier M38510/10107 (LM118)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM118 Cat. Min	LM118 Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS /101E Min	GEOS /101E Max	Units
*	V_{IO}	2/	25	-3	3	-4	4	-4	4	-4	4	mV
			-55/125	-4	4	-6	6	-6	6	-6	6	
*	$\frac{\Delta V_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25	-15	15	-	-	-25	25	-40	40	uV/°C
			25/125	-15	15	-	-	-25	25	-40	40	
	I_{IO}	2/	25/125	-40	40	{50 @ 25°C		-40	40	-40	40	nA
			-55/25	-80	80	{100 @ ΔT}		-80	80	-80	80	
*	$\frac{\Delta I_{IO}}{\Delta T}$	V_{CM} = 0 V	-55/25	-500	500	-	-	-1000	1000	-1000	1000	pA/°C
			25/125	-200	200	-	-	-1000	1000	-1000	1000	
	$+I_{IB}, -I_{IB}$	2/	25/125	1	250	{250 @ 25°C}		1	250	1	250	nA
			-55/25	1	400	{500 @ ΔT}		1	400	1	400	
*	V_{IO} Delta	3/	25	-.5	.5	-	-	-1	1	-1	1	mV
*	I_{IO} Delta	4/	25	-4	4	-	-	-	-	-	-	nA
	I_{IB} Delta		25	-25	25	-	-	-25	25	-25	25	nA
*	+PSRR, -PSRR	5/, 6/	25	0	100	-	-	-100	100	-100	100	uV/V
			-55/125	-	-	(70 dB Min)		-150	150	-150	150	
	CMR	6/	-55/125	80	-	80	-	80	-	80	-	dB
*	V_{IO} ADJ(+)	6/	-55/125	7.5	-	-	-	7	-	7	-	mV
	V_{IO} ADJ(-)		-55/125	7.5	-	-	-	-	-7	-	-7	
*	I_{OS} (+)	$\pm V_{CC}$=15 V, 7/ t ≤ 25 ms	25/125	-40	-12	-	-	-65	-	-65	-	mA
			-55/25	-55	-15	-	-	-65	-	-65	-	
*	I_{OS} (-)	$\pm V_{CC}$=15 V, 7/ t ≤ 25 ms	25/125	12	40	-	-	-	65	-	65	mA
			-55/25	15	55	-	-	-	65	-	65	

Table 5-4 (cont'd). Operational amplifier M38510/10107 (LM118)

	Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM118 Cat. Min	LM118 Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS /101E Min	GEOS /101E Max	Units
*	P_D	8/	-55	10	320	-	-	8/		8/		mW
			25	10	280	-	-					
			125	10	240							
*	I_{CC}	$\pm V_{CC}$=±15 V	-55	-	-	-	-	-	9	-	9	mA
		8/	25	-	-	-	8	-	8	-	8	
			125	-	-	-	7	-	7	-	7	
*	Z_{1S1}, Z_{1S2}		25	1	-	1	-	9/		9/		MΩ
			-55/125	0.5	-	-	-					
*	V_{op}	R_L = 10 KΩ	-55/125	34	-	-	-	±17	-	±17	-	V
		R_L = 2 KΩ		32	-	±12@V_{CC}=±15		±16	-	±16	-	
*	AVS (±)	R_L = 2 KΩ,	25	80	-	50	-	50	-	50	-	V/mV
		10 KΩ	-55/125	40	-	25	-	32	-	32	-	
*	AVS 10/	$\pm V_{CC}$ =±5 V, R_L = 2 KΩ	-55/125	40	-	-	-	10	-	10	-	V/mV
	TR (tr)	V_{IN} = 50 mV	-55/125	-	40	-	-	-		-	40	ns
*	TR (OS)	11/	-55/125	-	30	-	-	-		-	50	%
	BW	12/	-55/125	8.75	-	-	-	-	-	12/		MHz
*	SR(+),SR(-)	*13/V_{IN}=-5→ +5V Step	25/125	75	-	-	-	50	-	50	-	V/us
			-55	75	-	-	-	50	-	50	-	
	ts(+),ts(-)	14/	25	-	800	-	-	(Delete		-	800	ns
			-55/125	-	1200	-	-	Spec)		-	1200	
	CS		25	-	-	-	-	-	-	-	-	dB

Table 5-4 (cont'd). Operational amplifier M38510/10107 (LM118)

Parameter Symbol	Conditions 1/	T_A (°C)	/101D Spec. Min	/101D Spec. Max	LM118 Cat. Min	LM118 Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS /101E Min	GEOS /101E Max	Units
N1 (BB)	15/	25	-	-	-	-	-	25	-	25	uV rms
N1 (PC)		25	-	-	-	-	-	80	-	80	uV PK

NOTES:

1/ Unless otherwise specified, the supply voltages are $\pm V_{CC} = \pm 20$ VDC.

2/ This parameter is tested at $\pm V_{CC} = \pm 20$ V with $V_{CM} = 0$ V, -15 V and +15 V and also at $\pm V_{CC} = \pm 5$ V with $V_{CM} = 0$ V.

3/ These end point parameters are only measured following life and burn-in tests.

4/ I_{IO} Delta should be deleted because it represents a small change of a change and is difficult to measure, $\pm I_{IB}$ Delta should be sufficient.

5/ Amendment 1 corrected the 0 (Min) limit.

6/ In /101D, ±PSRR, CMR and V_{IO} ADJ were tested at 25°C only.

7/ JC-41 recommends that the short circuit be to ground instead of the opposite supply rail. GEOS recommends no change in the short to the rails, but a precautionary note should be added to indicate that I_{OS} protection at $T_A > 75°C$ cannot be guaranteed.

8/ It is recommended that P_D at $\pm V_{CC} = \pm 20$ V be replaced with I_{CC} at $\pm V_{CC} = \pm 15$ V.

9/ Parameters Z_{1S1} and Z_{1S2} should be deleted because they are not tested for in Table III and bias current limits over the common-mode range covers the DC input impedance (resistance).

10/ Test method change is recommended such that V_{IO} is not used in the AVS calculation.

Table 5-4 (cont'd). Operational amplifier M38510/10107 (LM118)

NOTES:

11/ Originally C_F = 0 and many vendors had trouble with this spec. JC-41 wanted to make C_F = 100 pF. GEOS data indicates that with C_F = 100 pF the device is masked. Instead GEOS recommends a limit change and C_F = 10 pF.

12/ GEOS recommends that this spec be deleted. It is calculated from 0.35/tr.

13/ JC-41 and GEOS recommend $\triangle$V points increased from ±1 V to ±2.5 V. SR(-) was specified at 50 V/us (Min).

14/ Periodic inspection only.

15/ New test circuit in /101E.

* Changed limits on test conditions between /101D and /101E.

SECTION VI

MIL-M-38510/102, VOLTAGE REGULATORS

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SECTION VI
MIL-M-38510/102

6.1 Background and Introduction

The voltage regulator specification /102 covers the detail requirements for a monolithic, silicon voltage regulator (commercial type 723). There were only two problems associated with the /102 specification when the contract effort began. First, the line-transient-response test limits could not be met by most manufacturers by a factor of 10, even though the limits were the same as those called out in the commercial specification. Second, the /102 specification was in need of clarification of the various test conditions, test circuit component values, test techniques and test parameters. Each test condition of /102 needed explicit definition.

6.2 Description of Device

The device specified by /102 is precision voltage regulator, equivalent to the commercial type 723. The device equivalent block diagram is shown in figure 6-1. Though used primarily for series regulator application, it can be operated with either positive or negative power supplies in series, shunt, switching, or floating modes. Several interconnection options are provided to extend the capability of the device in various applications. The internally generated reference voltage is buffered and brought out externally for use in a variety of connections. The inverting and non-inverting inputs of the error amplifier are brought out externally to allow for additional flexibility. The collector of the internal power transistor is separated from the internal circuitry and is brought out externally. An offsetting Zener diode is provided for minimum external parts count in floating configurations when using the DIP package versions. The device provides for limiting the output current by either linear or foldback methods.

6.2 Description of Device - (Continued)

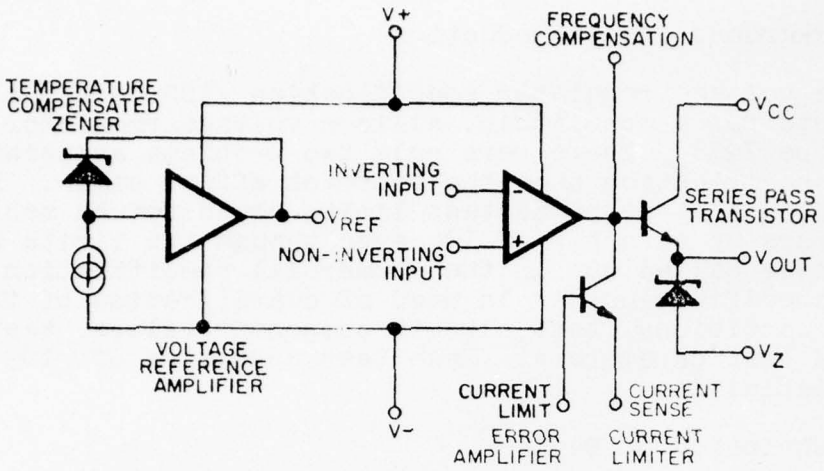
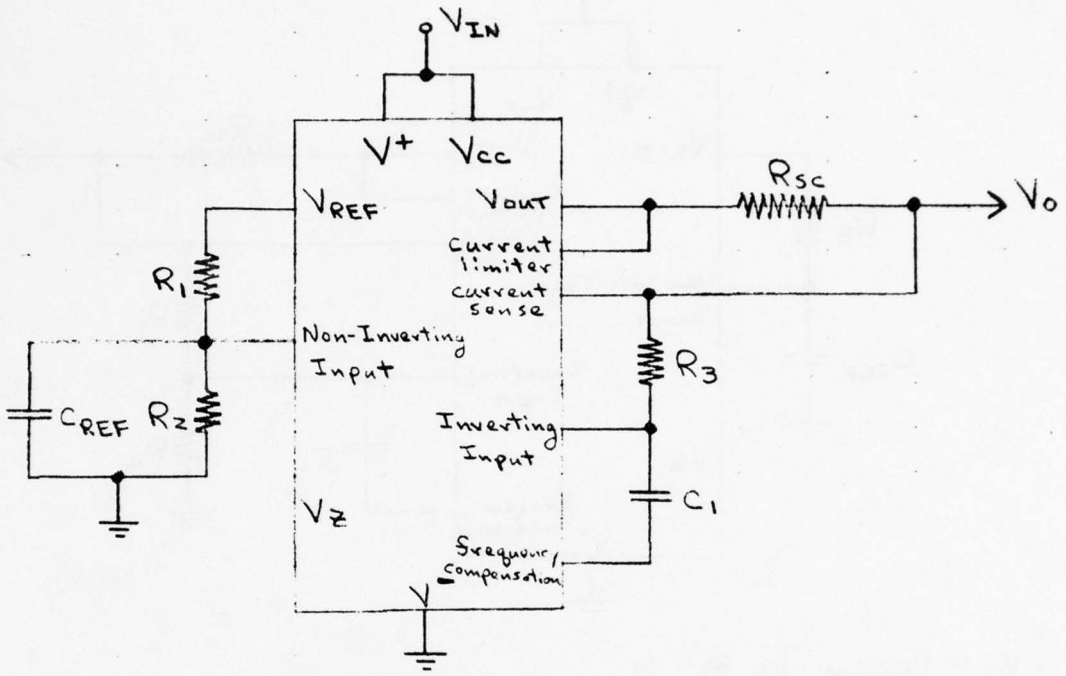


Figure 6-1. Device block diagram

The output voltage of the device, when used as a series regulator, is adjustable from 2 volts to 37 volts. The basic external circuitry for the device used in this mode is shown in figure 6-2 and 6-3. The device will supply output currents up to 150 milliamps without external pass transistors, but external transistors can be added to provide any desired load current. A capacitor (C1) is required to roll off the error amplifier and provide frequency compensation. An external resistor divider network is used to obtain the desired regulated output voltage. A capacitor (C_{REF}) is used to reduce the output voltage noise and ripple.

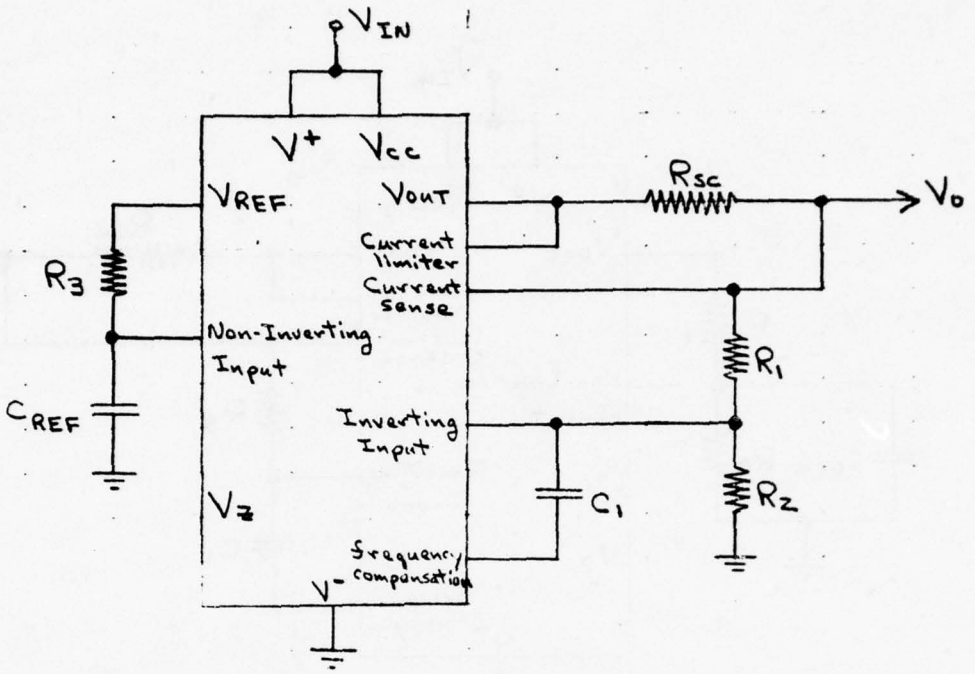


$$V_O = V_{REF} \times \frac{R2}{R_1 + R_2}$$

$$I_{REF} = \frac{VREF}{R_1 + R_2}$$

$$R_3 = \frac{R1 \times R2}{R_1 + R_2} \leq 10K \text{ Ohms}$$

Figure 6-2. Basic low-voltage regulator (V_O = 2 to 7 volts)



$$V_O = V_{REF} \times \frac{R1 + R2}{R_2}$$

$$R_3 = \frac{R1\ R2}{R1 + R2}$$

Figure 6-3. Basic high-voltage regulator (V_O = 7 to 37 volts)

6.3 Discussion

All of the original test limits of /102 were obtained from available commercial specification sheets. However, most manufacturers could not meet the line-transient-response test limits of /102 by a factor of 10. To alleviate this problem it was agreed to increase this limit from the original 1 millivolt/-volt to 10 millivolts/volt, and at the same time increase the rise and fall times of the line-transient pulse used in this test from the original value of 500 nanoseconds to 1 microsecond. Laboratory evaluation of devices from several manufacturers showed that most devices could meet the new test limit.

6.3 Discussion - (Continued)

Previously, the test conditions of /102 were not clearly defined, and could lead to correlation problems between test techniques. To alleviate this problem, /102 was revised so that all test conditions which could affect performance of the device are now explicitly defined.

6.4 Items for Future Consideration

The standard circuit schematic of the 723 has two NPN transistors with common collectors, the inverting transistor of the input differential pair and the current limit transistor. A user of the device reports that, since these transistors have common collectors, some manufacturers have designated them into the same epitaxial "tub". A lateral PNP injection can occur, if sufficient care is not taken to separate the base diffusions when the base-collector junction of the current limit transistor is forward-biased. The base-collector junction of the current limit transistor is routinely forward-biased when the device is used in the switching mode. The problem causes an artificially high base voltage on the inverting input transistor due to the lateral current flow from the current limit transistor base region. The /102 specification does not presently contain a test that will uncover this type of design problem. The manufacturers that had this problem with their devices were all from Canada and do not build the device anymore. In the future, a test to uncover this type of problem may have to be added to /102.

SECTION VII

MIL-M-38510/103, VOLTAGE COMPARATORS

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SECTION VII
MIL-M-38510/103 VOLTAGE COMPARATORS

7.1 Background and Introduction

The slash sheet for voltage comparators originated in 1972, was revised in 1973, and amended in 1974. The specification prior to this 1977 revision included four device types:

Device Type	Descriptive Name	Commercial Type
01	Voltage comparator	710
02	Dual comparator	711
03	Voltage comparator/Buffer	LM106
04	Voltage comparator	111

A major task in this characterization effort was to resolve problems within the spec for device type 04, the 111 comparator, and to incorporate the changes into revision B. An additional device type, the LH 2111 (dual 111) comparator, was also added to the /103 issue.

In this slash sheet, the 111 comparator is by far the most popular device from a user point of view, and most of the manufacturers were concerned only about curing the 111 ills. (One vendor also requested minor changes to device type 01 and 02.) At the end of 1976, there were no qualified sources for the 111 comparator. Even the inventor manufacturer made a point of this in a headline story in Electronics Buyer's News (Nov. 1, 1976), claiming that they had a "zero yield" to the existing spec.

Prior to this contractual effort, a proposed spec revision of /10304 was prepared at RADC and was issued via DESC to manufacturers and users (especially F16 Program users) for comments. This drawing, referred to as the "DESC Drawing" for the 111 and the dual 111 comparator, was delivered to GEOS along with comment letters from Advanced Micro Devices, Motorola, Texas Instruments, and National Semiconductor. During the next several months, many additional comments were received (mostly verbal) from attendees at JC-41 meetings. Data for forty-one 111 devices from two vendors taken on the Tektronix S3260 Test System at RADC, was later forwarded to GEOS. All of this information was reviewed, and the main effort centered upon revising the DESC drawing for the 111 comparator.

7.2 Device Description

The 111 comparator features very low input bias currents (100 to 200 nA max), a differential voltage range of ±30, a wide range of supply voltages (five volts single to ±15 volts dual), and high output voltage and current (50 volts, 50 milliamperes). A typical schematic is shown in figure 7-1.

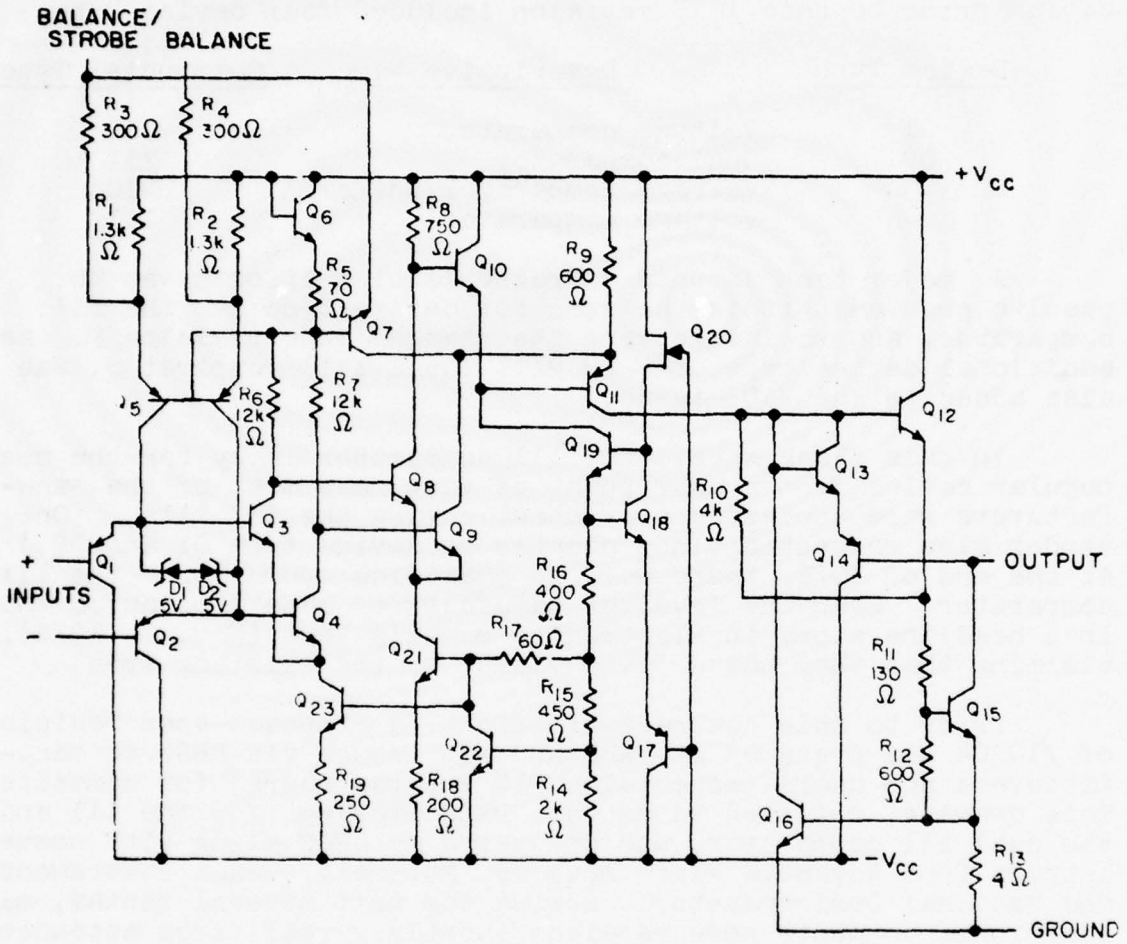

Figure 7-1. Typical schematic

The input differential stage (Q1, Q2) has a high emitter-base breakdown voltage in order to provide the ±30-volt differential input voltage. The current source which supplies the input stage bias can be raised to increase the input slew rate by connecting the BALANCE and BALANCE/STROBE terminals to $+V_{CC}$. Offset balancing can be achieved by connecting a potentiometer to these terminals, with the wiper connected through a resistor to $+V_{CC}$. The BALANCE/STROBE terminal can be used to

7.2 Device Description - (Continued)

strobe the device via an external transistor switch. The output can drive loads referenced to ground or to either supply. The emitter-follower output (pin 1) can be used to drive loads like lamps and relay coils; however, the device is difficult to stabilize in this configuration.

7.3 Table I Parameters and Limits

Extensive changes were required to the table I parameters and limits in order to characterize a more producible 111 comparator. Since there were no qualified sources for the part, user impact was not a driving force. Some of the users at the JC-41 meetings indicated that they perform their circuit designs using the industry data sheet (or the published catalog information). Some of the users may have based their designs upon the existing /103A, which has very tight limits on many parameters, and which also had some obvious errors. These users should have encountered great difficulty in procuring devices to that specification. For the (assumed) small number of such users, it is recommended that they reassess the impact of the new /103B limit changes on their designs.

Regarding the sources of information provided to GEOS (listed in 7.1) for this investigation, the following comments provide additional detail:

MIL-M-38510/103A	-	This formed the basis from which a new revision would be issued. Table I was not in good agreement with the test procedures of table III, and, in that sense, table I was misleading.
DESC Drawing	-	This document had already been circulated for comments, and provided a useful working spec, considerably improved over /103A. The rationale for limit changes was not known to GEOS, however.
Manufacturer Comment Letters	-	Many of the letters for the most part commented on the DESC drawing. Some manufacturers obviously had not done a thorough review and had very few comments at first. (Obvious errors in the comment copy were not recognized by these manufacturers.) There was not a great deal of consistency in the maker comments,

7.3 Table I Parameters and Limits

Manufacturer Comment Letters - (Continued)	-	(i.e., each was having his own particular difficulties) although there were certainly some common problems shared by all.
JC-41 Committee	-	This committee was very effective in resolving many of the differences among manufacturers, and in weeding out comments and complaints that had no validity. Through the process of open-table discussions, additional problems were identified and solved effectively. Considerable weight was placed on the committee decisions, since user, maker, government and GEOS took part in the resolution of the problems. Unfortunately, no data was provided by any of the manufacturers.
RADC Data	-	This data was taken on the Tektronix S3260 Test System. Much of it was taken at the three temperatures of interest (+125°C, 25°C, and -55°C). The majority of the data was taken on devices from one vendor (32 devices of 41). Of the 32 devices, 27 were of an older design that indeed showed many parameter failures. The new design from that vendor showed much better performance, but the sample was also very small (five pieces). Nonetheless, the data provided a source of information that could substantiate a problem with tight limits, but could not be used to verify limits, due to the small sample size.

7.3 Table I Parameters and Limits - (Continued)

RADC Report - Previous work performed by another characterization activity under contract F30602-74-C-0127, "Electrical Specification of Linear Integrated Circuits" was also reviewed, and the results of that effort were applied to the current characterization effort, where appropriate.

GEOS interfaces regularly with the Naval Weapons Support Center (NWSC) in Crane, Indiana concerning components for Fleet Ballistic Missile (FBM) equipments. The 111 comparator is presently procured for GEOS in accordance with NWSC drawing 3203068, "Specification for G-504 Microcircuits", which is in close agreement with 38510/103A. NWSC reports that there have been "massive problems on most Group A parameters. V_{IO}, I_{IO}, I_{IB}, etc were especially bad" referring to one vendor's parts. In a lot of 140 pieces procured from another major source, NWSC reported the following failures:

+25°C	+125°C	-55°C
8 A_{VC}	1 I_{IO}	17 V_{IO} adj-
3 V_{IO}	2 V_{IO}	2 V_{IO} adj+
3 V_{OL1}	(total of 3 units)	1 V_{OL3}
1 I_{CC}		1 V_{OL4}
(total of 13 units)		1 A_{VE}
		(total of 18 units)

This information was also considered in this investigation.

7.3.1 Comparison of Limits

Table 7-1 shows a comparison of limits obtained from several sources. The column heading "GEOS/103B" identifies the final GEOS recommendations for the new revision of 38510/103B. Table 7-2 is from /103B, table I.

7.3.2 Offset Voltage

Offset voltage is tested with split supplies (± 15 volts) over the common mode range, and over the temperature range; with a single supply (+5 volts) at zero common mode over the temperature range; at raised input current with dual supplies over common mode and temperature, for the total of 21 tests. Since offset does vary in all of these different configurations, it is necessary to perform the tests in order to guarantee performance.

Table 7-1. 111 Comparison

Parameter	Conditions $+V_{CC}$ = +15V Unless Otherwise Specified	1/ T_A (°C)	38510/103A Min	38510/103A Max
V_{IO}	R_S = 50Ω V_{IC} = 0, 13, -14.5V	25 -55 to 125	-2 -3	+2 +3
V_{IO}	R_S = 50Ω, V_{IC} = 0 $\pm V_{CC}$ = ±2.5V	25 -55 to 125	-2 -3	+2 +3
$V_{IO(R)}$	R_S = 50Ω V_{IC} = 0, 13, -14.5V $V_{BAL} = V_{BAL/STB} = +V_{CC}$	25 -55 to 125	-2 -3	+2 +3
$\Delta V_{IO}/\Delta T$	R_S = 50Ω	-55 to 125	-2	+2
I_{IO}	R_S = 100 KΩ V_{IC} = 0, 13, -14.5V	25 to 125 -55	-10 -15	+10 +15
$I_{IO(R)}$	R_S = 100 KΩ V_{IC} = 0V $V_{BAL} = V_{BAL/STB} = +V_{CC}$	25 to 125 -55	-10 -15	+10 +15
$\Delta I_{IO}/\Delta T$	R_S = 100 KΩ	25 to 125 -55	-20 -50	+20 +50
$+I_{IB}$	R_S = 50Ω V_{IC} = 0 V_{IC} = -14.5V	25 to 125 -55 25 to 125	-100 -125 -100	0 0 0
$-I_{IB}$	(Same as above for $+I_{IB}$)	-55	-125	0
$V_{O(STB)}$	R_S = 50Ω I_{STB} = -3.0 mA	-55 to +125	-	-
CMR	R_S = 50Ω V_{IC} = 13, -14.5V	-55 to +125	80	-

Table 7-1. 111 Comparison

Orig. LM111		DESC Dwg.		JC-41		GEOS /103B		
Min	Max	Min	Max	Min	Max	Min	Max	Units
-3 -4	+3 +4	-2 -3	+2 +3	-3 -4	+3 +4	-3 -4	+3 +4	mV mV
- -	- -	-2 -3	+2 +3	-3 -4	+3 +4	-3 -4	+3 +4	mV mV
- -	- -	-2 -4	+2 +4	Delete		-3 -4.5	+3 +4.5	mV mV
-	-	-25	+25	-25	+25	-25	+25	µV/°C
-10 -20	+10 +20	-10 -15	+10 +15	-10 -20	+10 +20	-10 -20	+10 +20	nA nA
- -	- -	-25 -50	+25 +50	Delete		-25 -50	+25 +50	nA nA
- -	- -	-70 -150	+70 +150	-100 -200	+100 +200	-100 -200	+100 +200	pA/°C pA/°C
-100	0	-100	+0.1	-100 @25°C	+0.1	-100	+0.1	nA
-150	0	-125	+0.1	-150 @-55/125°C	+0.1	-150	+0.1	nA
-100	0	-100	+0.1	-150 @25°C	+0.1	-150	+0.1	nA
-150	0	-125	+0.1	-200 @-55/125°C	+0.1	-200	+0.1	nA
-	-	14	-	14	-	14	-	V
-	-	80	-	80	-	80	-	dB

Table 7-1. 111 Comparison - (Continued)

Parameter	Conditions +Vcc = +15V Unless Otherwise Specified	1/ T_A (°C)	38510/103A	
			Min	Max
I_O	+Vcc = + 18V $\overline{V}_O$ = 32$\overline{V}$ V_{IO} = 5 mV	-55 to +25 125	0 0	100 100
I_G	+Vcc = +18V $\overline{V}_O$ = 32$\overline{V}$	-55 to +25 125	-100 -100	0 0
I_{I1}	+Vcc = +18V $\overline{V}_{ID}$ = -$\overline{29}$V	-55 to +125	0	20
I_{I2}	+Vcc = +18V $\overline{V}_{ID}$ = +$\overline{29}$V	-55 to +125	0	20
$+I_{CC}$		-55 +25 +125	0 0.5 0.5	6 4 6
$-I_{CC}$		-55 +25 +125	-3 -4 -5	0 -0.5 -0.5
I_{OS}	10 ms, max	-55 +25 +125	120 70 50	200 170 130
P_D	(Calculation)	-55 +25 +125		
$V_{IO(ADJ)+}$ $V_{IO(ADJ)-}$	R_S = 50Ω	25 to 125 -55	10 10	- -
V_{OL1} V_{OL2}	+Vcc = +4.5V -Vcc = 0 V_{ID} = -6 mV I_O = 8 mA	-55 to +125 and V_{IC}=-1.75V V_{IC} = +0.75V	0 0	0.4 0.4

Table 7-1. 111 Comparison - (Continued)

Orig. LM111		DESC Dwg.		JC-41		38510 /103B		
Min	Max	Min	Max	Min	Max	Min	Max	Units
0 0	10 500	0 0	10 500	0 @ 25°C 0 @ 125°C	10 500	0 @ 25°C 0 @ 125°C	10 500	nA nA
- -	- -	-10 -100	0 0	Delete		Delete		µA µA
-	-	0	20	0	500	0	500	nA
-	-	0	20	0	500	0	500	nA
- - -	- 6 -	0.5 0.5 0.5	6 5 4	0 0 0	7 6 6	0 0 0	7 6 6	mA
- - -	- 5 -	-5 -4 -3	-0.5 -0.5 -0.5	-6 -5 -5	0 0 0	-6 -5 -5	0 0 0	mA
Curve 120 Typ. @ 25° C		120 70 50	250 200 150	0 0 0	250 200 150	0 0 0	250 200 150	mA
- - -	- 165 -	15 15 15	165 135 105	Delete		Delete		mA
- -	- -	5 5	- -	5 25°C Only	-	5 25°C Only	-	mV
0 0	0.4 0.4	0 0	0.4 0.4	0 V_{IC} = +2.25 Delete	0.4	0 V_{IC} = +2.25 Delete	0.4	V

Table 7-1. 111 Comparison - (Continued)

Parameter	Conditions +VCC = +15V Unless Otherwise Specified	1/ T_A (°C)	38510/103A	
			Min	Max
V_{OL3} V_{OL4}	+VCC = +15V V_{ID} = -5.0 mV I_O = 50 mA	-55 to +125 and V_{IC} = 13V V_{IC} = -14V	0 0	1.5 1.5
$\pm A_{VC}$	30V 1 KΩ Load	+25 -55 to +125	200 150	- -
$\pm A_{VE}$	R_L = 600Ω	+25 -55 to +125	50 40	- -
t_{RLHC}	V_{OD} = -5 mV C_L = 50 pF V_{IN} = 100 mV	-55 to +25 +125	- -	300 300
t_{RHLC}	V_{OD} = +5 mV C_L = 50 pF V_{IN} = 100 mV	-55 to +25 +125	- -	300 300
t_{RLHE}	V_{OD} = +5 mV C_L = 50 pF VIN = 100 mV	-55 to +25 +125	- -	800 800
t_{RHLE}	V_{OD} = -5 mV C_L = 50 pF VIN = 100 mV	-55 to +25 +125	- -	1300 1300

NOTE:

1/ Temperature range grouping may not be consistent from all specification sources.

Table 7-1. 111 Comparison - (Continued)

Orig. LM111		DESC Dwg.		JC-41		GEOS /103B		Units
Min	Max	Min	Max	Min	Max	Min	Max	
0	1.5	0	1.5	0	1.5	0	1.5	V
@ 25°C		0	1.5	V_{IC} = 0		V_{IC} = 0		
V_{IC} = ?		0	1.5	V_{ID} = -6 mV		V_{ID} = -6 mV		
				Delete		Delete		
200	Typ.	150	-	80	-	80	-	V/mV
-	-	35	-	35	-	35	-	
-	-	50	-	Delete		10		V/mV
-	-	10	-			8	-	
-	200	-	300	-	300	-	300	nS
-	Typ.	-	500	-	600	-	600	
	-							
-	180	-	300	-	300	-	300	nS
-	Typ.	-	450	-	600	-	500	
	-							
-	500	-	800	Delete		Delete		nS
-	Typ.	-	2500					
	-							
-	800	-	1300	Delete		Delete		nS
-	Typ.	-	3500					
	-							

Table 7-2. Electrical performance characteristics for device types 04 and 05

Characteristic	Symbol	Conditions		Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$R_S = 50\Omega$; V_{IC} = 0V, 13V and -14.5V	$T_A = 25°C$	-3.0	+3.0	mV
			$-55°C \leq T_A \leq +125°C$	-4.0	+4.0	mV
		$R_S = 50\Omega$; V_{IC} = 0V; $\pm V_{CC} = \pm 2.5V$	$T_A = 25°C$	-3.0	+3.0	mV
			$-55°C \leq T_A \leq +125°C$	-4.0	+4.0	mV
Raised input offset voltage	$V_{IO(R)}$	$R_S = 50\Omega$; V_{IC} = 0V, 13V and -14.5V; $V_{BAL} = V_{BAL/STB} = +V_{CC}$	$T_A = 25°C$	-3.0	+3.0	mV
			$-55°C \leq T_A \leq +125°C$	-4.5	+4.5	mV
Input offset voltage temperature coefficient	$\Delta V_{IO}/\Delta T$	$R_S = 50\Omega$		-25	+25	$\mu V/°C$
Input offset current	I_{IO}	$R_S = 100\ k\Omega$; V_{IC} = 0V, 13V and -14.5V	$25°C \leq T_A \leq +125°C$	-10	+10	nA
			$T_A = -55°C$	-20	+20	nA
Raised input offset current	$I_{IO(R)}$	$R_S = 100$ k ; V_{IC} = 0V; $V_{BAL} = V_{BAL/STB} = +V_{CC}$	$25°C \leq T_A \leq$ [illegible]°C	-25	+25	nA
			$T_A = -55°C$	-50	+50	nA
Input offset current temperature coefficient	$\Delta I_{IO}/\Delta T$	$R_S = 100\ k\Omega$	$25°C \leq T_A \leq 125°C$	-100	+100	PA/°C
			$-55°C \leq T_A \leq +25°C$	-200	+200	PA/°C
Input bias current	$+I_{IB}$	$R_S = 50\Omega$; V_{IC} = 0V	$25°C \leq T_A \leq 125°C$	-100	+0.1	nA
			$T_A = -55°C$	-150	+0.1	nA
		$R_S = 50\Omega$; V_{IC} = 13V and -14.5V	$25°C \leq T_A \leq 125°C$	-150	+0.1	nA
			$T_A = -55°C$	-200	+0.1	nA
	$-I_{IB}$	$R_S = 50\Omega$; V_{IC} = 0V	$25°C \leq T_A \leq 125°C$	-100	+0.1	nA
			$T_A = -55°C$	-150	+0.1	nA
		$R_S = 50\Omega$; V_{IC} = 13V and -14.5V	$25°C \leq T_A \leq 125°C$	-150	+0.1	nA
			$T_A = -55°C$	-200	+0.1	nA
Collector output voltage (STROBED)	$V_{O(STB)}$	$R_S = 50\Omega$; I_{STB} = -3.0 mA		14		V
Common mode rejection	CMR	$R_S = 50\Omega$; V_{IC} = 13V and -14.5V		80		dB
Output leakage current	I_{CEX}	$\pm V_{CC} = \pm 18V$; V_O = 32V	$T_A = 25°C$	0	10	nA
			$T_A = 125°C$	0	500	nA
Input leakage current	I_{I1}	$\pm V_{CC} = \pm 18V$; V_{ID} = -29V		0	500	nA
	I_{I2}	$\pm V_{CC} = \pm 18V$; V_{ID} = +29V		0	500	nA

Table 7-2. Electrical performance characteristics for device types 04 and 05 - Continued.

Characteristic	Symbol	Conditions		Limits Min	Limits Max	Unit
Positive supply current (Limit is for one comparator of device type 05)	$+I_{CC}$		$T_A = -55°C$		7.0	mA
			$T_A = 25°C$		6.0	mA
			$T_A = 125°C$		6.0	mA
Negative supply current (Limit is for one comparator of device type 05)	$-I_{CC}$		$T_A = -55°C$	-6.0		mA
			$T_A = 25°C$	-5.0		mA
			$T_A = 125°C$	-5.0		mA
Output short circuit current	I_{OS}	10 ms maximum test duration	$T_A = -55°C$	0	250	mA
			$T_A = 25°C$	0	200	mA
			$T_A = 125°C$	0	150	mA
Adjustment for input offset voltage	$V_{IO(ADJ)+}$	$R_S = 50\Omega$	$T_A = 25°C$	5.0		mV
	$V_{IO(ADJ)-}$	$R_S = 50\Omega$	$T_A = 25°C$	5.0		mV
Low level output voltage	V_{OL1}	$+V_{CC} = +4.5V$; $-V_{CC} = 0V$; $V_{IC} = 2.25V$ $V_{ID} = -6.0$ mV; $I_O = 8$ mA		0	0.4	V
	V_{OL2}	$\pm V_{CC} = \pm 15V$; $V_{ID} = -6.0$ mV $V_{IC} = 0V$; $I_O = 50$ mA		0	1.5	V
Voltage gain (collector output)	$\pm A_{VC}$	$V_O = 30V$ through 1.5 kΩ load	$T_A = 25°C$	80		V/mV
			$-55°C \leq T_A \leq 125°C$	35		V/mV
Voltage gain (emitter follower output)	$\pm A_{VE}$	$R_L = 600\Omega$	$T_A = 25°C$	10		V/mV
			$-55°C \leq T_A \leq +125°C$	8		V/mV
Response time - low-to-high level - collector output	t_{RLHC}	V_{OD} (overdrive) = -5 mV; $C_L = 50$ pF minimum $V_{IN} = 100$ mV	$-55°C \leq T_A \leq 25°C$	0	300	ns
			$T_A = +125°C$	0	600	ns
Response time - high-to-low level - collector output	t_{RHLC}	V_{OD} (overdrive) = +5 mV; $C_L = 50$ pF minimum $V_{IN} = 100$ mV	$-55°C \leq T_A \leq 25°C$	0	300	ns
			$T_A = 125°C$	0	500	ns

7.3.2 Offset Voltage - (Continued)

The RADC data revealed a high incidence of failures (50 to 100 percent) on this parameter under all conditions, for the first submittals from one vendor. A small sample of a redesigned part showed very few failures. The NWSC data reinforced the case for an increase in limits. JC-41 made the recommendation for three millivolts at 25°C and four millivolts over temperature. Applying the temperature drift limit of 25 uV/°C x (125 - 25°C) = 2.5 mV, one could argue the case for a limit over temperature of 3 mV + 2.5 mV = 5.5 mV. Another argument against a tighter limit at 25°C is that military systems have to be designed for the complete temperature range. There is no need to constrain the maker to a tighter limit since the user has to use the temperature limits. While this rationale may be valid for many applications, there are military applications where severe temperature environments are not encountered and the designer may estimate a "poor case" rather than a "worst case" parameter limit.

The raised offset voltage limits are another issue. JC-41 recommended that these tests be deleted since the manufacturers do not believe that anyone uses the part in the raised configuration. Nonetheless, the configuration is shown in the vendor catalogs, and is listed among the features of the device, so that a designer may have used it, or may anticipate using it. Two makers wanted the limit increased; one observed that an increase of one millivolt was typical in the raised configuration.

In consideration of all of the above arguments, the limits shown under the column heading "GEOS/103B" are the final recommendations for offset voltage tests.

7.3.3 Offset Voltage Drift

The test limit for offset voltage temperature drift in 38510/103A is ± 2 µV/°C. This limit is totally unreasonable for the 111 comparator, and may have been an error in the printing. Previous characterization done under contract F30602-74-C-0127 included analysis of data on 50 pieces. A recommendation of ± 25 µV/°C was made in that effort. The DESC drawing and the JC-41 committee agreed to the limits, and, therefore, the present recommendation incorporated into /103B is ± 25 µV/°C.

7.3.4 Input Offset Current

The input offset current is not consistently specified in tables I and III of /103A. Table I shows a limit of 15 nanoamperes (nA), whereas table III shows a limit of 10 nanoamperes at 25°C and 15 nanoamperes at the temperature extremes. The 25°C limit was judged to be too tight by two vendors; one requested a limit of 12 nA, the other wanted a limit of 15 nA.

7.3.4 Input Offset Current - (Continued)

However, the catalog limit is 10 nA, and three major vendors were satisfied with leaving the limit at 10 nA. The limit was not changed at 25°C, therefore.

At 125°C, the input offset current is typically less than the value at 25°C, since the input bias currents decrease with increasing temperature. One vendor stated that a redesigned 111 comparator which they developed did not show this trend, and could even increase with increasing temperature. This could change the character of the part. It was finally concluded that a separate limit could be added at a future date for the particular schematic of the redesigned part, when the device is ready to be qualified. The 125°C limit was therefore chosen to be equal to the 25°C limit. Even though it will be somewhat less at 125°C, there is no apparent advantage to the user to select a lower limit at the high temperature.

The current at -55°C can be as much as twice that at 25°C. Applying the coefficient of offset current temperature drift yields a current change of 20 nA in the temperature range of -55°C to +25°C. The JC-41 Committee reported that the limit of 15 nA was too tight for this device, and the limit was relaxed to the catalog value of 20 nA for the temperature range of -55°C to +25°C.

When the input is "raised", the input bias current more than doubles. Revision /103A does not take this into account. JC-41 recommended elimination of this parameter in the raised configuration. In accordance with the rationale for raised V_{IO} (previously stated), the parameter was retained, but with realistic limits previously determined for the DESC drawing, as shown in table 7-1.

7.3.5 Input Offset Current Drift

As was the case for input offset current, the drift limits in /103A were excessively tight, and not realizable for the 111 comparator. Previous characterization effort resulted in the DESC drawing recommendation of 70 picoamperes (pA) per°C for the hot temperature range, and 150 pA/°C for the cold temperature range. These limits were still not adequate in the judgment of the JC-41 Committee. They required 100 pA/°C for the hot range, and (by the 2 to 1 ratio), 200 pA/°C for the cold range. Since this is still a very low drift and is also a difficult measurement at these very low currents, the request was granted.

7.3.6 Input Bias Current

There was no contention for the /103A limit of 100 nA at 25°C for the input bias current. The cold temperature limit was a problem to the manufacturers, and a small change probably won't impact the average user. Table I of /103A was incorrect in that it showed only the limit of 125 nA, and was not consistent with table III. A small increase from 125 nA to 150 nA at -55°C was granted. As per the previous discussion on I_{OS}, the hot limit remains the same as the room temperature limit.

7.3.7 Strobe Current

The test for strobe current was originally run by measuring that value of current flowing out of the strobe terminal required to establish an output voltage (high) of 14 volts minimum in the presence of an input drive signal of -5 mV. The DESC drawing changed the test philosophy by forcing the strobe sink current to a known value (-2 mA) and measuring an output voltage of 14 volts, minimum. This method is superior because it matches the application, which essentially consists of a current sink to zero volts at the strobe terminal. The DESC drawing called for a current of two milliamperes. This is not sufficiently large at -55°C to ensure a "high" output state. The value of three milliamperes is required. It should be noted that a user cannot use the strobe circuit shown in vendor catalogs (which is a transistor switch with a one kilohm emitter resistor to zero volts driven by a TTL gate), since a worst case logic "1" is 2.4 volts, minimum, which yields a current sink of less than two milliamperes. A resistor value must be selected which guarantees three milliamperes sink at the strobe terminal.

7.3.8 Output Leakage Current

The test limit for output leakage current stated in /103A is 100 nA at all temperatures, with 18-volt supplies with an input of five millivolts and with an output voltage of 32 volts. The catalog specs are 10 nA at 25°C and 500 nA at the temperature extremes. The DESC drawing recommends the same limits. There is a problem in measuring the leakage current at the low temperature of -55°C due to external leakage paths (e.g., frost). It is known that the leakage current at the low temperature will always be less than the leakage current at room temperature. Therefore, the recommendation was made to delete the measurement at -55°C.

7.3.9 Ground Current

The test circuit for the 111 comparator is especially difficult to stablize due to the very high gain and bandwidth of the device. It is even more of a problem when the output emitter-follower configuration is used. For this reason, and

7.3.9 Ground Current - (Continued)

also because ground current is not an important design parameter to the user, the parameter was deleted from the requirements of /103B for the 111 comparator and the dual 2111 device.

7.3.10 Input Leakage Current

The input leakage currents are measured in order to verify that the input stages have a breakdown voltage higher than $\pm$ 29 volts. If the front end has already passed its other tests (such as input offset voltage and current), then the only parameter left to be verified is the breakdown differential input voltages. The choice of limits is therefore not to identify a precise leakage current limit, but rather to determine whether or not the devices can support the differential voltage. A limit suggested by the JC-41 Committee was adopted, which is 500 nA, maximum. It is understood that the actual leakage is much less than 500 nA, and that this larger limit is for measurement convenience only.

7.3.11 Supply Currents and Power Dissipation

The supply current limits were changed to reflect the requirements of the devices. The limits in /103A, table III, were apparently reversed for the -55°C and +125°C tests, for $-I_{CC}$. In the new revision, the minimum values were also changed to zero so that a minimum current is not a requirement. If a device is open, it will obviously fail other tests. Power dissipation was dropped from table I since it was a simple calculation that offered no additional information.

7.3.12 Output Short Circuit Current

The maximum values of output short-circuit current were changed in the previous characterization effort and the minimum values were retained. The JC-41 Committee recommended that the minimum limits be dropped, since there is no apparent reason why a minimum short-circuit current has to be guaranteed. This recommendation was accepted. The changes in maximum value were also accepted since there is not penalty to the user, and some devices do fail the former /103A maximum limits.

7.3.13 Adjustment for Input Offset Voltage

The limits for $V_{IO(ADJ)}$ have been particularly troublesome. The /103A was 10 millivolts (mV), and the test was performed at all temperatrues. A general guideline for this parameter is to select a value which is one millivolt greater than the offset voltage to be compensated. The JC-41 Committee recommended the same value as that determined in the previous characterization effort (5 mV), and JC-41 also recommended performing the test at 25°C only. The V_{IO} limit is 3 mV at 25°C, so the adjust range of 5 mV would also include the effects of input offset current multiplied by the source resistance (20 nA x 100K = 2 mV). The test is performed with only 50 ohms of source resistance but a user may well choose higher values. The limit of 5 mV is therefore a reasonable one from that point of view. The NWSC data shows failures at all temperatures for this parameter to a limit of 5 mV, however. This parameter is worst at the low temperatures. Most user applications would do the offset adjust at room temperature or with elevated temperature due to normal circuit dissipation. Therefore, the recommendation to delete offset adjust except at 25°C was accepted. It is anticipated that some yield loss will occur at 5 mV, but it should be tolerable.

7.3.14 Low Level Output Voltage

Both /103A and the DESC drawing specified four tests (V_{OL1} - V_{OL4}) for output voltage saturation, over both temperature and common mode voltage. This quantity of testing is unreasonable for this parameter. JC-41/GEOS recommendations are for one test at low supply (+4.5 volts) at each temperature, and a second tests at + 15 volts at maximum output current (50 milliamperes), again at each temperature. For the single supply test, a common mode voltage of 2.25 volts is applied; for the dual supply test, the common mode voltage is zero. For the 8-mA output, /103A had specified a 6-mV input drive; yet for the 50-mA output, only a 5-mV input differential voltage was specified. For /103B, JC-41 recommended a 6-mV input drive for each test, in order to ensure that output saturation is achieved.

7.3.15 Voltage Gain (Collector Output)

Voltage gain is a difficult parameter to test, since the high gain/high bandwidth comparator has a tendency to oscillate in the nulling test circuit. The test limits in /103A were high: 200 V/mV minimum at room temperature, and 150 minimum over the temperature range. The DESC drawing relaxed the limits somewhat to 150 minimum at room temperature, and 35 minimum over the temperature range. The JC-41 Committee requested a further relaxation of the room temperature limit to 80 minimum. A gain of 80,000 V/V is still very adequate for most applications, and since a user would have to consider temperature

7.3.15 Voltage Gain (Collector Output) - (Continued)

effects, he would be restrained to a lower overall limit anyhow. The change to 80 V/mV was therefore granted for the 25°C limit. There was no disagreement by anyone for the change to 35 V/mV, minimum, over temperature.

7.3.16 Voltage Gain (Emitter Output)

Most of the manufacturers wanted to delete the test for the emitter output voltage gain, for the reason that the test circuit was impossible to stabilize in this mode. One vendor claimed that there should be no difficulty, although care had to be exercised. GEOS felt that the output does exist, and, therefore, it should be tested. A limit change was made to relieve some of the difficulty, as shown in table 7-1. At the time of this writing, there is still difficulty reported by manufacturers, and this decision should be readdressed in a future effort.

7.3.17 Response Time, Low-to-high Level, Collector Output

The response time test has been a problem chiefly at the high temperature condition. Data from one manufacturer showed a typical 1.5 to 2.0 times increase beyond the value for the 25°C test condition. All manufacturers agreed via JC-41 that the high temperature limit had to be changed since it was a major detriment to yield. The original 25°C limit of 300 nanoseconds (ns) was acceptable to all concerned parties, and a proposed change to 600 ns for the temperature range was also agreed upon for the low-to-high transition. The DESC drawing had also modified the response time test circuit by adding a shunt output capacitance of 50 pF to account for strays, probe and test jig capacitance, etc., and also to aid the user to applying the device with capacitive loading. Errors on the waveforms in figure 9 of /103A were also corrected in this revision.

7.3.18 Response Time, High-to-low Level, Collector Output

The same comments apply here as for the above parameter, except the recommended change for the limit at high temperature is 500 ns instead of 600 ns.

7.3.19 Response Times, Emitter Output

The tests for emitter output response time were deleted, due to the difficulty in establishing a stable test circuit in the emitter output configuration. Further, the device is considerably slower in this configuration and should only be used to drive low-speed loads such as relays, lamps, etc. The test limit proposed by DESC for this parameter was 3500 ns over temperature at +125°C.

7.3.20 Table I Limit Change for Device /10302

One manufacturer requested a limit change to the 711 comparator, device /10302. The parameter in question is t_{HTHR} the response time of the output in a high-to-low transition resulting from a 100-mV step with a 5-mV overdrive at the input. Data supplied by this manufacturer included data on his own devices plus samples from another manufacturer. The data showed that a limit of 60 ns, maximum, for this response time was not compatible with the capabilities of the device. The current sink capability of the 711 is only 0.5 mA, compared to 2.0 mA for the 710, and 50 mA for the 111 comparator. The test circuit in /103A did not specify any value for output capacitance, although some capacitance always exists in a test circuit. A value of 5 pF was recommended; the value must be small enough not to mask the device characteristics, and large enough to account for strays. The test limit of 90 ns was selected based upon limited data and recommendations from one manufacturer. This is a low useage part in comparison to the 111 comparator, and only one or two manufacturers are interested in becoming qualified to supply the part.

7.4 Test Circuit

The test circuit for static and dynamic tests was not evaluated during this effort. The DESC drawing had included several changes which had been reviewed by the manufacturers and which had received a majority approval. Some of the vendors have general difficulty achieving stability with this test circuit, and they claim that the 111 comparator was not intended to be operated in a linear mode, which the nulling circuit does impose. The problem, previously discussed, is the stability of a high-gain, high-bandwidth device. One manufacturer reported that he was developing an alternate test circuit which he planned to propose to JC-41; however, this has not been completed to date. If difficulty with the test circuit continues, it should be reevaluated in a future effort.

Since the issuance of /103B, two additional changes to the test circuit became necessary. The input source resistors of 100K ohms had to be changed to 50K ohms to accomodate the increased maximum input bias current of 200 nA. (200 nA x 100K x 1000 = 20 V, which exceeds the output swing of the null amplifier in the test circuit). The second change involved the addition of a relay to break the wired connection of 50K-ohm resistors to ground at each input. This shunt resistance interferes with the input leakage test. The relay will open the shunt path to make the measurement valid. These changes will be incorporated in an amendment to /103B.

7.5 Burn-in Circuit

The 111 comparator burn-in circuit was designed to achieve burn-in at maximum output current. However, in figure 3 of /103A, a load resistor of 300 ohms is specified for the burn-in circuit. Since the output swings between +15 volts and -15 volts, with the load returned to -15 volts, the output current approaches 100 mA. The rated output current is 50 mA. Consequently, the burn-in circuit was modified, changing the 300-ohm resistor to 620 ohms.

Another change made to the burn-in circuit was to reduce the input drive from $\pm$ 15 V p-p at 1 KHz to $\pm$ 8 V p-p at 1 KHz, which is more readily mechanized with standard bench test equipment. The decreased input voltage does not now represent the maximum input stress, although maximum output stress is maintained.

One manufacturer recommended that the burn-in circuit be changed to one of maximum output voltage stress at very low output current. At high temperature, sodium contamination on the die surface will penetrate the oxide layer and affect junction breakdown, leakage, etc. This recommendation was not incorporated, although it should be reconsidered in a future effort.

7.6 Table IV Operating Life Deltas

The end point electrical parameters selected for the 111 comparator in /103A were V_{IO}, I_{IO}, I_{IB}. The delta limit on I_{IO} was 1.5 nA. In essence, this represents a delta of a delta, since I_{IO} is calculated from the difference of the two input bias currents. The 1.5-nA measurement is also directly affected by the measurement accuracy and the repeatability, since it is made over a 1000-hour life test period and may even be measured on different instruments. Therefore, the I_{IO} delta was deleted from table IV, and a requirement was added to measure both input bias currents (instead of one bias current and a delta). The maximum bias current was tightened from 125 nA to 100 nA to agree with table I. An additional parameter, output leakage, was added to table IV with a delta limit of $\pm$ 5 nA, at the recommendation of a major manufacturer. The V_{IO} delta limit was retained without change.

In /103B, table II, the group C and D endpoint electrical parameters test requirements were modified to include subgroup 1 tests for class B and class D devices. The previous revisions required only the table IV deltas, which is not a sufficient check after a 1000-hour life test.

7.7 Recommendations for Future Effort

Slash Sheet 103B is presently being amended to incorporate minor changes previously discussed in this section. Future effort could be applied to address other troublesome areas which may still penalize the yield and, therefore, the cost of these devices. The following is a brief list of suggested topics for future effort on slash sheet 10304,-05:

- Consider alternates to the existing test circuit which would be less prone to oscillations.
- Consider an alternate burn-in circuit that would detect sodium ion contamination more readily (high voltage and high temperature at low output current).
- Consider alternate methods to verify the emitter output performance. Present test configurations are difficult to stabilize.
- Survey user need for the raised configuration; delete tests if there is no user need.
- Consider addition of an emitter output leakage test for increased reliability.

SECTION VIII

MIL-M-38510/10404

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SECTION VIII

MIL-M-38510/10404

DUAL DIFFERENTIAL LINE RECEIVER

8.1 Background and Introduction

MIL-M-38510/10404 has been issued for a few years. All of the manufacturers were having trouble meeting the requirements especially input current low for the strobe and response control inputs.

8.2 Description of Device Type

The particular device being investigated is a dual differential line receiver commercially called 9615.

8.3 Discussion

The vendor exceptions to I_{IL2} and I_{IL3} limits were studied in great detail. Two of the manufacturers requested changes to the present limits. The third manufacturer, when contacted, admitted to having problems with the same limits.

The problem stems from the fact that the manufacturers, when settling the present limits, did not consider all the current paths which determine the limits over the temperature range. After discussing the problem thoroughly with the manufacturers, the following limits were agreed upon:

I_{IL2} -1.0 mA min to -2.4 mA max

I_{IL3} -1.7 mA min to -4.1 mA max

AD-A052 357 GENERAL ELECTRIC CO PITTSFIELD MASS ORDNANCE SYSTEMS F/G 9/5
ELECTRICAL CHARACTERIZATION OF LINEAR INTEGRATED CIRCUITS.(U)
FEB 78 J S KULPINSKI, J YAPLE, R PASKOWSKY F30602-76-C-0345
UNCLASSIFIED RADC-TR-78-22 NL

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SECTION IX

MIL-M-38510/108, TRANSISTOR ARRAYS

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SECTION IX

MIL-M-38510/108, TRANSISTOR ARRAYS

9.1 Background and Introduction

The purpose of this task was first of all to investigate the vendor exceptions to the present specification and, secondly. to investigate the two areas of major concern to the manufacturers (i.e., channel separation and gain bandwidth).

9.2 Description of Device

This specification covers monolithic NPN transistor arrays. These transistors can be used in a variety of applications and are specified as general purpose transistors as well as matching characteristics.

9.3 Discussion

The following list is submitted to give recommendations for changes in the present specification in answer to vendor exceptions:

Page 3	Add Note 10 to collector to emitter voltage, $V_{CE(sat)}$.
Page 4	For temperature coefficient of input offset voltage change 15 uV/°C to 25 uV/°C.
Page 5	Add footnote 10 limits for Q_4 of Type 01 should be .55 volt max at -55°C and 25°C and .80 volt max at 125°C.
Page 16	In Figure 7 change t_s to be from 1.8 volts input to 1.4 volts of output.
Page 17	Figure 9 add Note 5. Other circuit configurations or commercially available equipment is acceptable if the accuracy can be proven.
Page 18	Test No. 37 change $V_{CE(sat)}$ from .400 volt max to .55 volt max.
Page 20	Test No. 88 change $V_{CE(sat)}$ from .600 volt max to .800 volt max.
Page 20	Test No. 105 change 15 uV/°C to 25 uV/°C.
Page 21	Test No. 129 change 15 uV/°C to 25 uV/°C.

9.3 Discussion (Continued)

Page 21	Add to footnote No. 14 except for qualification only CQ1 shall be measured.
Page 26	Test No. 123 change 15 uV/°C to 25 uV/°C.
Page 27	Test No. 160 change 16 uV/°C to 25 uV/°C.
Page 28	Add to footnote No. 2 except for qualification only CQ1 shall be measured.

9.3.1 Channel Separation

The channel separation test was cited as a very difficult test to perform even as a sample test. The test basically called for one transistor Q_A to be pulsed on while another transistor Q_B (with its base and emitter grounded) was monitored at its collector, which was pulled up to V_{CC}. The specified limit was 80 decibels and a two-volt, five-microsecond pulse with five-nanosecond edges was applied to the base of Q_A. Therefore, the test man was asked to look for a 200-microvolt pulse on the collector of Q_B. Several problems are encountered due to the low level of the maximum allowed output pulse. First, any common impedance back to the supply return causes an apparent pulse to appear at the output. Second, the supply voltage itself responds to the load variation and develops perturbations at the rising and falling edges of the pulse. Third, the steep edges (less than five nanoseconds) applied to the base of Q_A are capacitively coupled to the collector of Q_B, which tends to confuse the test man into thinking that these perturbations are what this test limit is directed at. (See figure 9-1 showing edge perturbations at V_{CC} and collector of Q_B.) In fact, the test man should be looking for an attenuated five-microsecond pulse. Since the channel separation is much better than 80 decibels for the applied pulse, no hint of such a pulse can be seen.

Due to the difficulties described above and since parasitic capacitance (which this test is directed toward) will degrade the gain-bandwidth product, f_t, which is presently tested. it was recommended that the channel separation test be deleted.

9.3.2 Gain Bandwidth (f_t)

The f_t test circuit is based upon MIL-STD-750, Method 3306, and has been in common use for many years. Admittedly, 100 megahertz measurements are difficult to perform, and layout precautions are necessary on the test equipment and test socket.

9.3.2 Gain Bandwidth (Continued)

Commercially available or home-built test circuits are acceptable if correlation can be demonstrated.

An f_t circuit, based upon the MIL-STD method, was constructed in the Components Engineering Lab. After some initial adjusting of lead lengths and layout, the circuit performed adaquately and readings were repeatable. The gain was checked on commercial equipment and gave similar results.

The conclusion is that the f_t test circuit as stated can be reproduced and used without great difficulty.

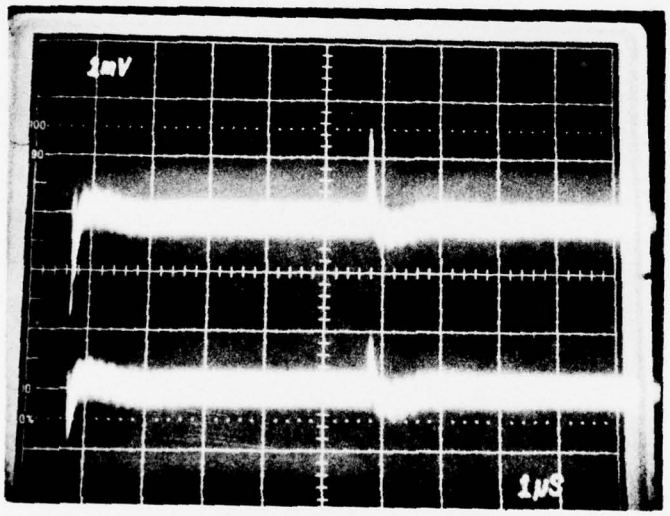

Figure 9-1. Pulse perturbations

9.4 Items for Future Consideration

Changes to be considered are:

1) Adding circuit layout to Figure 9 for gain-bandwidth product.
2) Drop channel separation test as stated. If test remains, a new test method will have to be developed.

SECTION X

MIL-M-38510/107A, VOLTAGE REGULATORS, POSITIVE

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SECTION X

MIL-M-38510/107A, VOLTAGE REGULATORS, POSITIVE

10.1 Introduction and Background:

The specification, MIL-M-38510/107, for three-terminal, positive-voltage regulators was initially signed off on 1 June 1973. The original specification, however, only listed requirements for the five-volt regulator, LM109. Revision A of /107 added positive voltage regulators from two newly developed regulator families. These were the 78xx/78Mxx families and the LM140K-xx/LM141H-xx families.

The following table shows the voltage regulators included in this specification from these families:

Table 10-1. Device types specified

Device Type	Output Voltage, V	Output Current, A	Commercial Type
02	5	0.5	78M05, LM141H-05
03	12	0.5	78M12, LM141H-12
04	15	0.5	78M15, LM141H-15
05	24	0.5	78M24, LM141H-24
06	5	1.0	7805 , LM140K-05
07	12	1.0	7812 , LM140K-12
08	15	1.0	7815 , LM140K-15
09	24	1.0	7824 , LM140K-24

The new devices employ current limiting, short circuit protection and thermal shutdown to protect both the regulator and the equipment serviced by it. In addition, the unusual startup voltage required by the LM109 is not required by either of the two newly developed families.

GEOS activities began by distributing preliminary copies of MIL-M-38510/107A to interested users and to manufacturers of the new voltage regulators for their comments. The response from several manufacturers was excellent and extensive. Because of the degree to which the specification was reviewed, it was not surprising that conflicting opinions existed in the type of tests performed, in the test circuits and in the parameter tolerances. These conflicting opinions resulted in several iterations to the slash sheet until finally the document was thoroughly reviewed by the JC-41 Committee on Voltage Regulators. The comments by the JC-41 Committee

were reviewed, suggested tests and test circuits were examined and a final slash sheet was developed that was both consistent with the high reliability philosophy of MIL-M-38510 and acceptable to all reviewing agencies.

10.2 Device Description and Operation

The 7800 and LM140 three-terminal, positive-voltage regulator families each have distinctive design. However, the commonality of performance between these two families allows a single procurement specification to be used for both.

The positive-voltage regulator families specified in /107A generally contain the same functional elements. A general block diagram of the regulator is shown in figure 10-1. The voltage regulator consists of: (a), a start-up circuit to insure that the device is rapidly brought into regulation, (b), a temperature-compensated voltage reference with a current source to eliminate the effect of the unregulated input voltage, (c), an error amplifier, (d), a thermal shutdown circuit, (e), a series pass regulating transistor, and, (f), resistor trims to set the regulated output voltage and the peak output current.

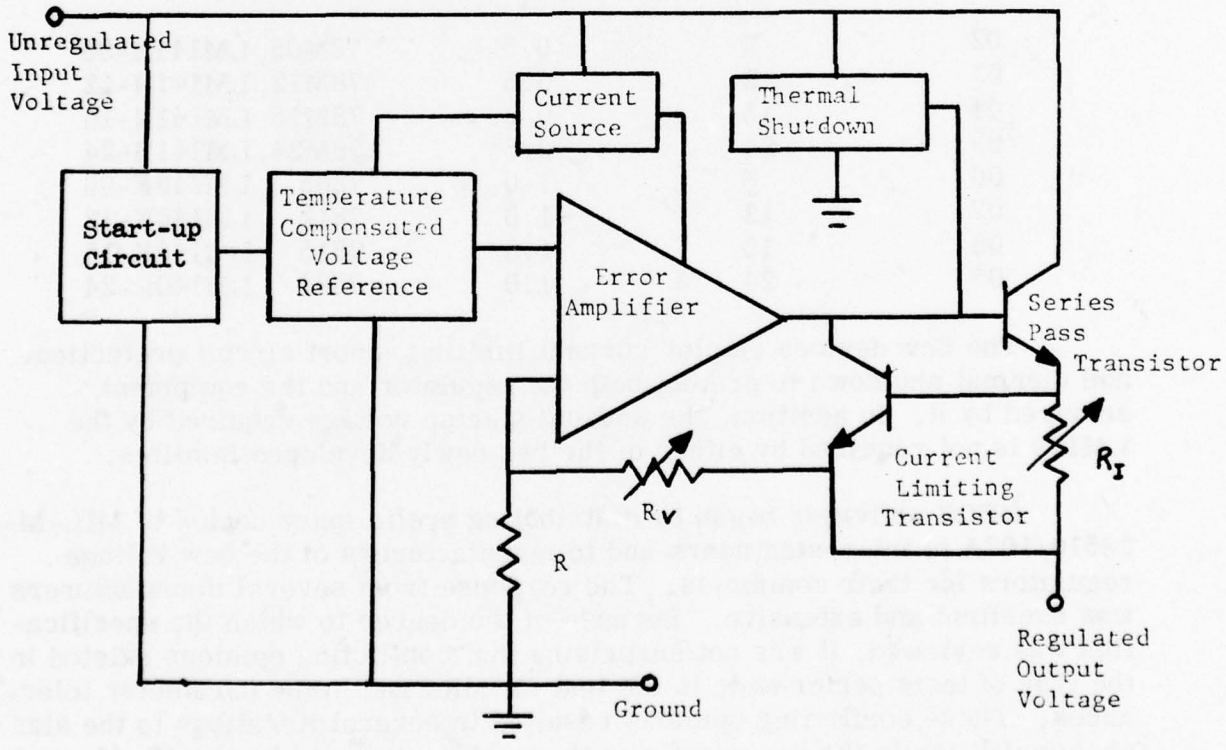
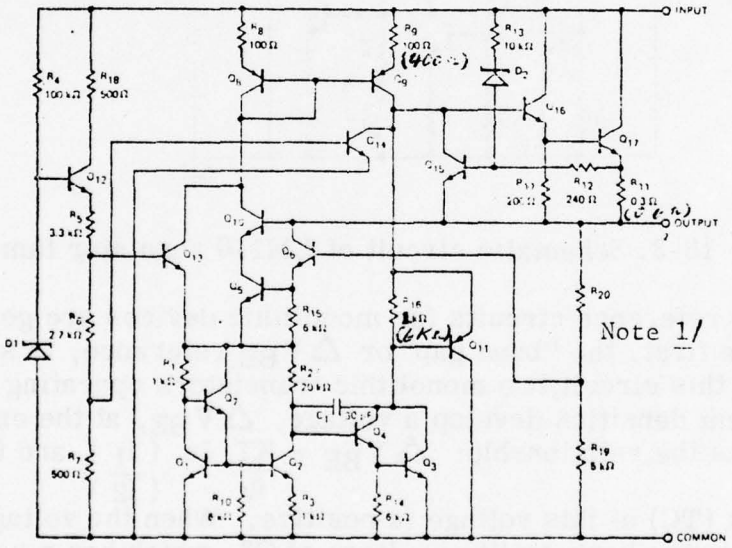


Figure 10-1. Block diagram of the voltage regulator

A detailed schematic of the 78xx and 78Mxx voltage regulators is shown in figure 10-2 and the schematic for the LM140K-xx and LM141H-xx voltage regulators is shown in figure 10-3. A startup circuit for the 78xx and 78Mxx family consists of Q12, Q13 and D1. Upon application of the input voltage, current flows through the Q12 circuit, and through the circuit consisting of Q8, Q9 and Q13. The startup circuit provides the internal voltage reference circuit with adequate supply current to rapidly bring it into regulation.



Notes:
1. R_{20} = 0 to 25K ohms, depending on nominal output voltage.
2. Resistor values in parentheses are for 78Mxx series.

Figure 10-2. Schematic circuit of 7800 regulator family

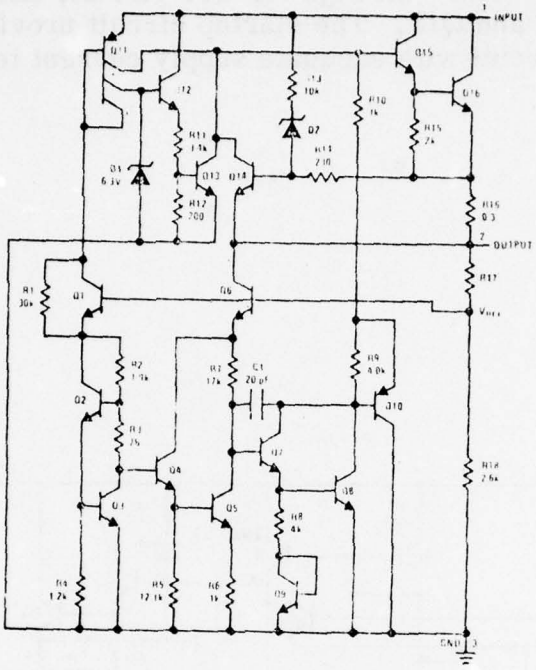


Figure 10-3. Schematic circuit of LM140 regulator family

Voltage reference circuits for monolithic devices are generally of two types. The first, the "band gap" or ΔV_{BE} reference, is shown in figure 10-4. In this circuit, two monolithic transistors operating at different collector current densities develop a voltage, ΔV_{BE}, at the emitter of Q2. This voltage has the relationship: $\Delta V_{BE} = \frac{KT}{q} \ln \left(\frac{I_1}{I_2} \right)$ and the temperature coefficient (TC) of this voltage is positive. When the voltage is amplified and added to the base-emitter voltage of Q3, which has a negative TC, the resultant output is:

$$V_{REF} = V_{BE3} + \frac{R2}{R1} \Delta V_{BE}.$$

By proper adjustment of the gain (R_2/R_1), the negative TC of V_{BE3} can be made to cancel the positive TC of ΔV_{BE}. The result is a voltage reference that has nearly zero temperature drift.

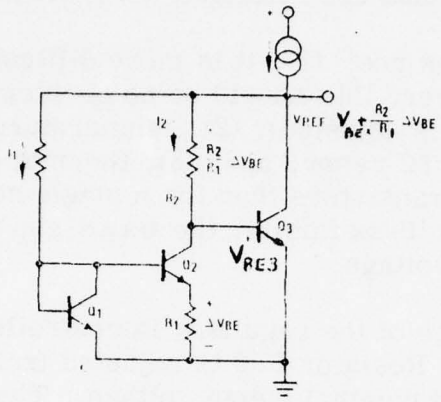


Figure 10-4. Band gap reference

The second type of voltage reference is the "buried zener" shown in figure 10-5. The major drawback of a standard zener reference, poor long-term stability, is eliminated when the site for zener breakdown is placed below the die surface. This shields the breakdown junction from the effects of mobile ion surface contamination. Presently, construction of this device is possible only with a new technology known as ion implantation.

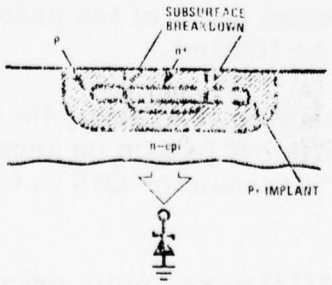


Figure 10-5. Buried zener diode reference

The advantages of the band gap reference over the zener reference are: (1), low noise, since the band gap reference operates as a normal linear circuit and since avalanche breakdown devices such as zeners are inherently noisy, and, (2), better long-term stability, since P-N junction voltages are very stable and are relatively insensitive to surface effects.

The disadvantages are: (1), it is more difficult to control the initial voltage tolerance (however, this should be no problem with these regulators since the output voltage is adjusted), (2), temperature drift is usually higher than that of a good zero TC zener, and, (3), thermal gradient effects are more severe for three transistors than for a single zener diode. In both the 78xx family and the LM140-xx family, the band gap reference is used to provide a stable output voltage.

The output voltage of the regulator is controlled by the ratio of two resistors R20 and R19. Resistor R20 is adjusted from 0 to 25K ohms depending on the desired nominal output voltage. The output voltage is determined by the relationship:

$$V_{OUT} = (V_{REF}) \cdot \frac{(R_{19} + R_{20})}{(R_{19})}$$

The device has three mechanisms - thermal shutdown, current limiting and short circuit protection - that are used to provide both long-term and short-term protection. The temperature sensing element is a transistor, Q14, which is biased with approximately +0.4 volt across the base-emitter junction. As the die temperature increases, the V_{BE} required to turn on the transistor decreases. At a temperature above 150°C, but below 205°C, the transistor fully turns on. This removes the base current from Q16 which in turn turns off the pass transistor Q17.

The current limiting circuit consists of a series output resistor, R11, and transistor, Q15. As the current through R11 increases, the base-emitter voltage of Q15 also increases. When the output current increases to the range of two to four amperes, the voltage drop, V_{R11}, is sufficient to turn on transistor Q15. This will shunt some of the pass transistor base current and cause the output current to be limited.

When the output is shorted to ground, the voltage across the input to output terminals may be sufficient to turn on zener diode D2. This will provide adequate base current to transistor Q15 to turn it on; thus turning off the pass transistor, Q17.

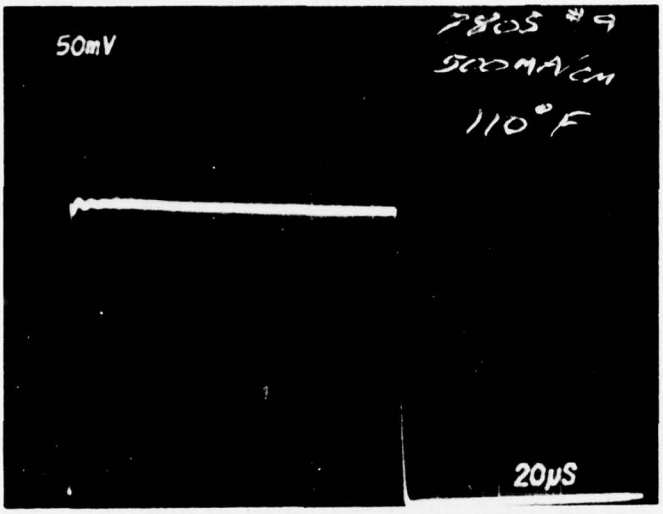
The LM140K-xx/2M141H-xx family provides the same protection.

The major elements in this design are:

thermal shutdown	-	Q13
current limit	-	R16, Q14
short circuit protection	-	R13, D2, Q14

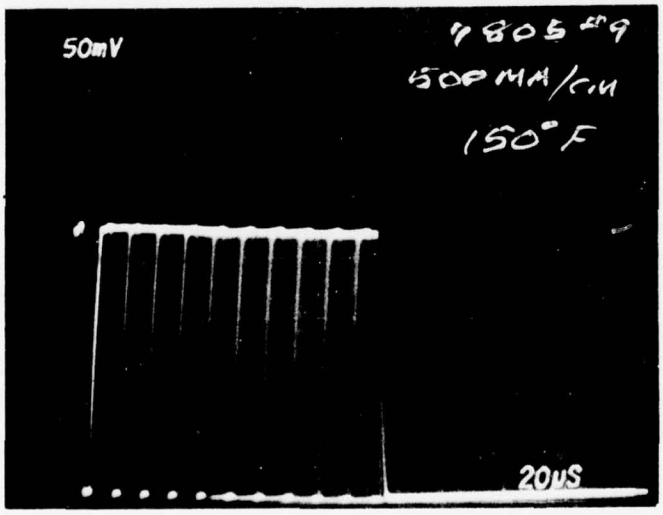
The three protection circuits are interactive and, as the device operation changes from one mode of protection to another, oscillations in the output current are very apt to occur. Figure 10-6 shows Peak Output Current versus Temperature. The input voltage to the device was 10 volts, dc. The load current is pulsed to force the device into current limit. As shown in figure 10-6a, the peak output current is approximately 2.5 amperes. Under the heavy load current conditions established in this test, the base-emitter junction of Q15 is conducting. As the device case temperature, (T_C), increases, the output voltage for this device decreases. (This temperature characteristic was described in detail in an earlier report, dated 23 August 1975.) In addition, the transistor betas increase, and thermal run away can occur in transistor Q15. When this occurs, transistor Q15 saturates, the pass transistor, Q17, turns off and the base current to Q15 is shut off. The result is that local heating due to conduction through the pass transistor circuit is stopped. As the device cools, transistor Q15 comes out of saturation and re-establishes the peak output current level. Local heating begins, and the cycle repeats. Figure 10-6b shows the current oscillations that can occur in the current limit mode of operation.

As the device case temperature is further increased, the thermal shutdown transistor, Q14, starts to turn on. This causes the pass transistor, Q17, to turn off, decreasing the output current and reducing the local heating of the device. With the local heating effect reduced, the oscillations stop. Figures 10-6c and 10-6d show the output current, without oscillation, at two different case temperatures. Figure 10-6e shows the oscillations that occur as the input voltage is increased. This causes additional local heating in the pass transistor circuit so that oscillations can occur at a lower case temperature. Figure 10-6g shows the peak current output of a different manufacturer's device. The oscillations in this device were linear and had a frequency of several megahertz. Since these anomalies all occurred during the current limit mode of operation, they do not present a problem to normal operation.



a. T_C = 110°F (43.3°C)

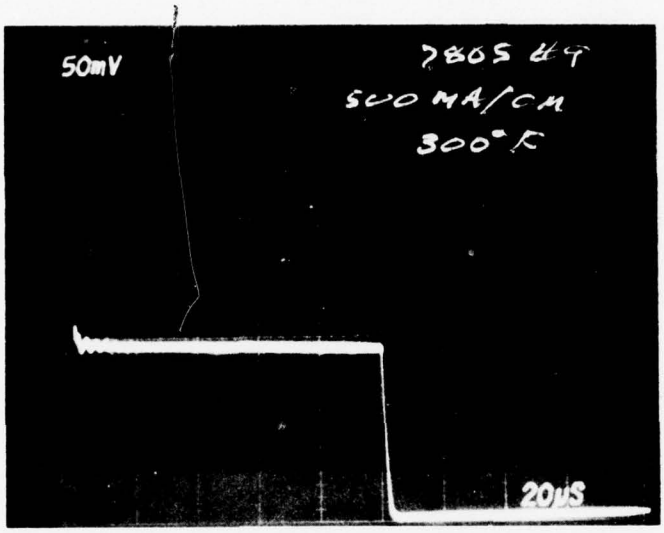
V_{in} = 10 VDC



b. T_C = 150°F (65.5°C)

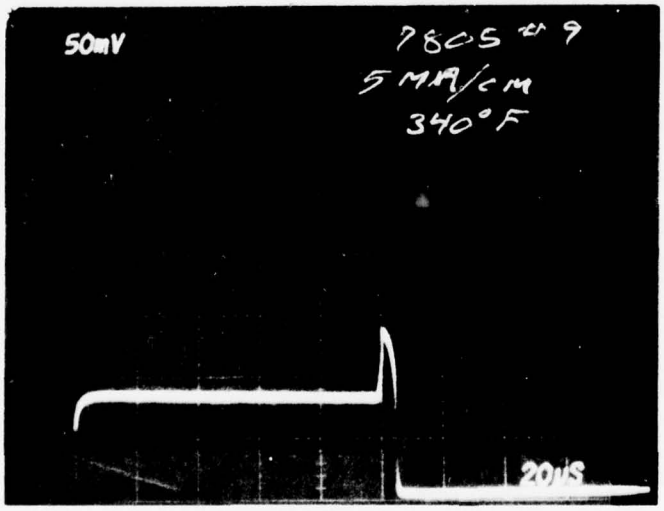
V_{in} = 10 VDC

Figure 10-6. Peak current output versus temperature



c. T_C = 300°F (148.8°C)

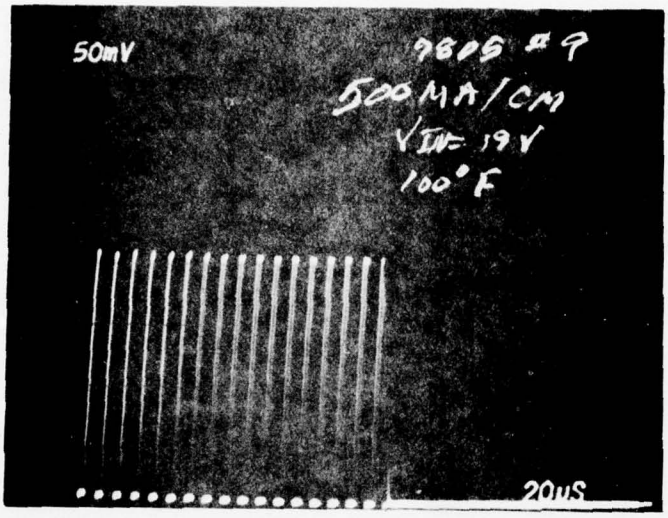
V_{in} = 10 VDC



d. T_C = 340°F (171.1°C)

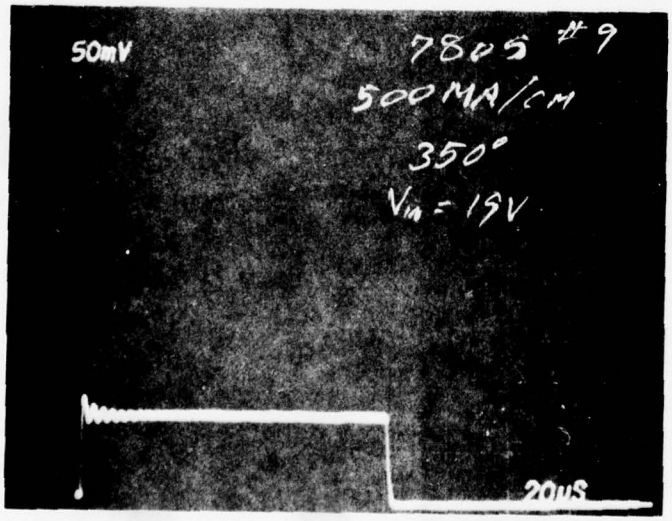
V_{in} = 10 VDC

Figure 10-6 (cont'd). Peak current output versus temperature



e. T_C = 100°F (37.7°C)

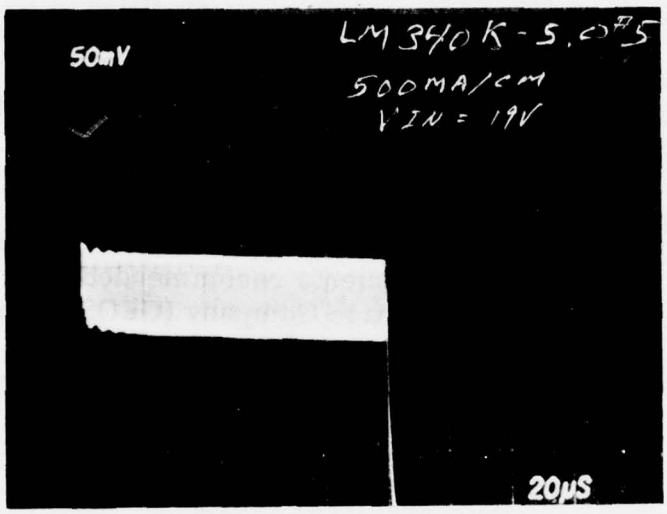
V_{in} = 19 VDC



f. T_C = 350°F (176.6°C)

V_{in} = 19 VDC

Figure 10-6 (cont'd). Peak current output versus temperature



g. T_C = 77°F (26°C)

V_{in} = 19 VDC

Figure 10-6 (cont'd). Peak current output versus temperature

10.3 Electric Parameters and Limits

Basically, the test parameters specified in the last recommended revision A are the same as those listed in first recommended revision A as received by the General Electric Company. However, the number of tests specified for several of the 100 percent parameters was increased at the suggestion of the JC-41 Committee. In addition, the startup voltage test was considered unnecessary from the manufacturer's view point and undesirable from the user's view point. Also, the thermal shutdown test was considered uneconomical as it was originally proposed. For these reasons, the startup test was deleted and the thermal shutdown requirements were modified.

Further, modifications were made to the format to change the document from four device types, each having two different case sizes and output current requirements, to eight distinct device types. This leads to greater flexibility and makes it easier to add new devices to the specification. Tables 10-2 through 10-9 list the parameters for device types 02 through 09, respectively. The tables show a comparison between the parameter requirements as received and the final parameter requirements recommended by Ordnance Systems Department of the General Electric Company (GEOS). The final recommendations shown in these tables represent the parameters and limits agreed to by all members of the JC-41 Committee on Voltage Regulators.

10.4 Burn-in Circuit

The voltage regulators specified in slash sheet 107 represent a recent innovation in power monolithic devices. These devices contain several overstress protection circuits, one of which is a thermal shutdown circuit. The thermal shutdown circuit is designed to turnoff the output pass transistor whenever the device temperature exceeds the temperature threshold range (150°C to 205°C). Because of the thermal shutdown action, both the accelerated burn-in and the accelerated operating life tests at elevated temperatures were deleted.

A pre-burn-in test was added in which the device operates in an output short circuit mode for four hours without a heat sink. The temperature rise under these conditions is sufficient to cause the device to heat up to the normal thermal shutdown temperature. Under these conditions, devices that do not shut down will be destroyed. Following the pre-burn-in test, a standard burn-in test is run at a temperature of 125°C. Minor changes were made to the burn-in circuit to reduce the number of components required to test the eight device types. The original burn-in test circuit required eight different load resistors for the eight device types. The final recommended test circuit requires four different load resistors for the eight device types.

The pre-burn-in and the standard burn-in test circuits are shown in figures 10-7 and 10-8, respectively.

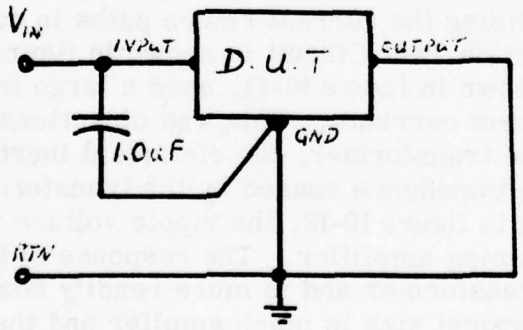


Figure 10-7. Pre-burn-in test circuit

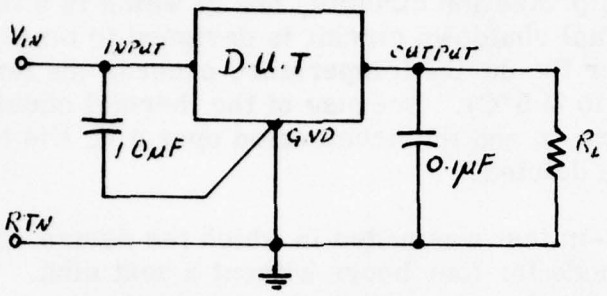


Figure 10-8. Burn-in and operating life test circuit

10.5 Test Circuits

Generally, all of the test circuits were modified because either the circuit was unsatisfactory or the test limits were modified requiring modification to the test circuit. The original test circuit for measuring the general static parameters is shown in figure 10-9. This circuit was felt to be unsatisfactory because the load circuit transistor has a low beta which would cause measurement errors. As a replacement for this, the final version, shown in figure 10-10 specifies a Darlington transistor device with much higher beta values. In addition, better load current control is achieved by combining the Darlington transistor in a feedback amplifier circuit and measurement correlation is improved by defining the current return paths in each test circuit.

The Ripple Rejection Test Circuit is shown in figures 10-11 and 10-12. The original version, shown in figure 10-11, used a large transformer capable of carrying large direct currents. This was objectionable because of the large physical size of the transformer, the electrical inertia of the transformer and the high source impedance caused by the transformer d-c resistance. In the test circuit shown in figure 10-12, the ripple voltage is combined with the d-c voltage in a summing amplifier. The response of this circuit is much faster than that of the transformer and is more readily adapted to automatic test equipment. The physical size is much smaller and the source impedance is essentially zero.

The Noise Test Circuit, shown in figure 10-13, is the same circuit as proposed in the original specification.

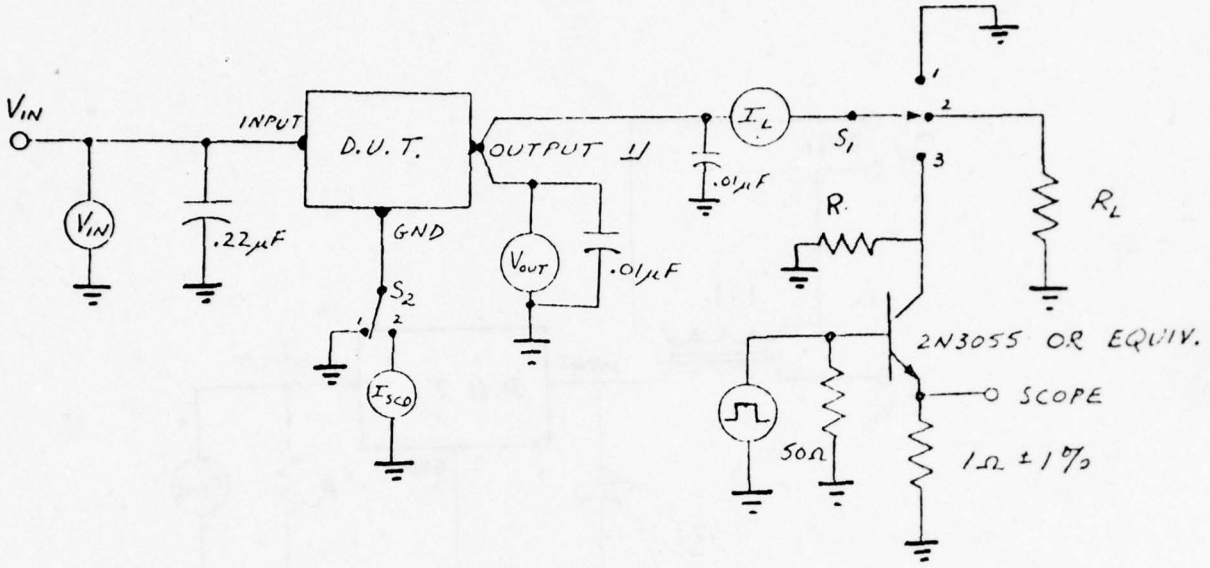


Figure 10-9. Original version of test circuit for static tests

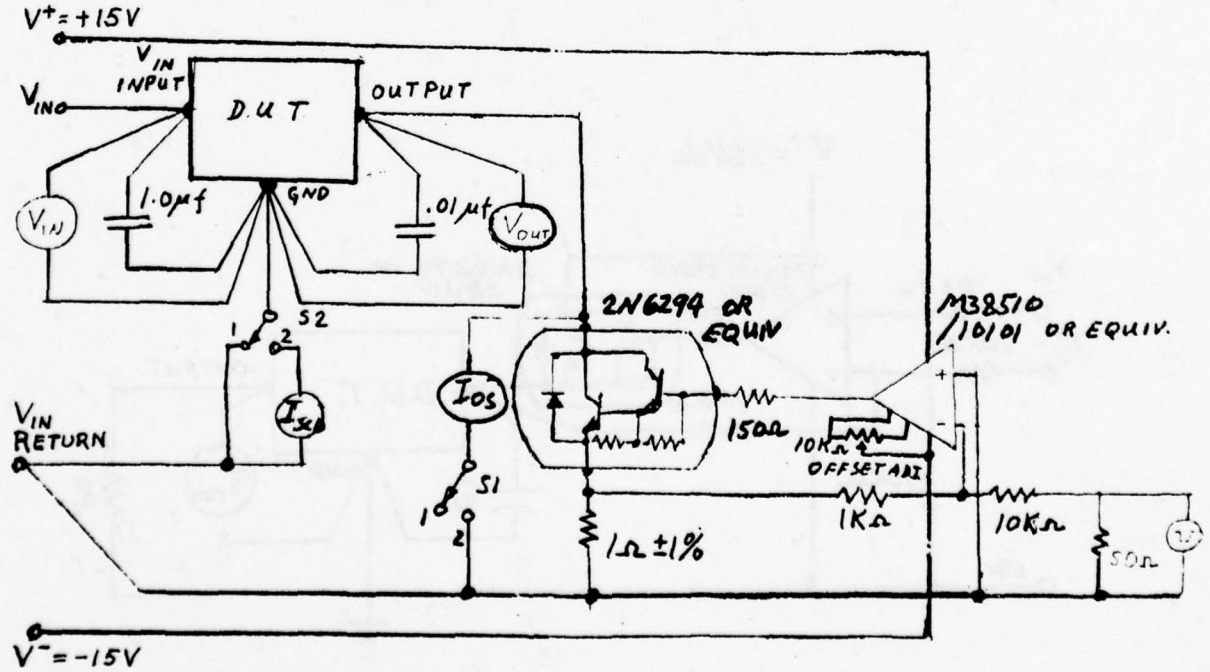


Figure 10-10. Final version of test circuit for static tests

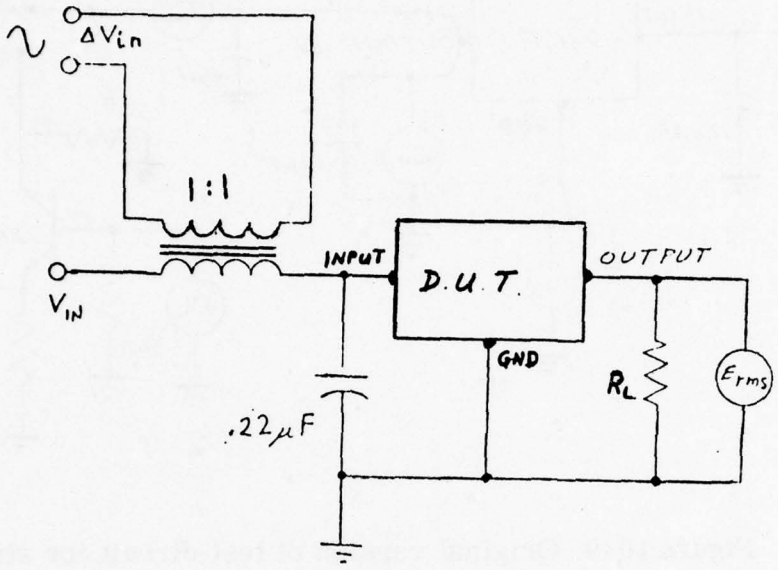


Figure 10-11. Original version of ripple rejection test circuit

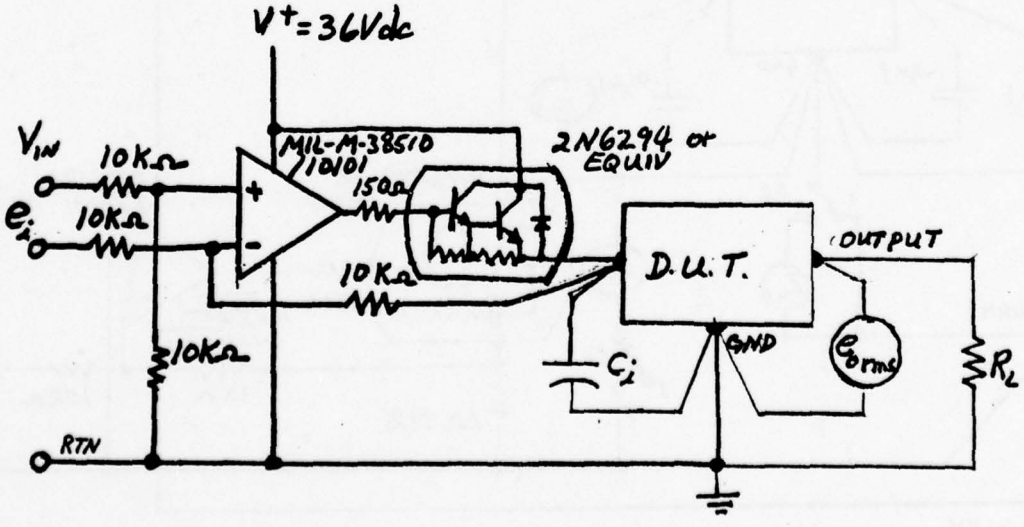


Figure 10-12. Final version of ripple rejection test circuit

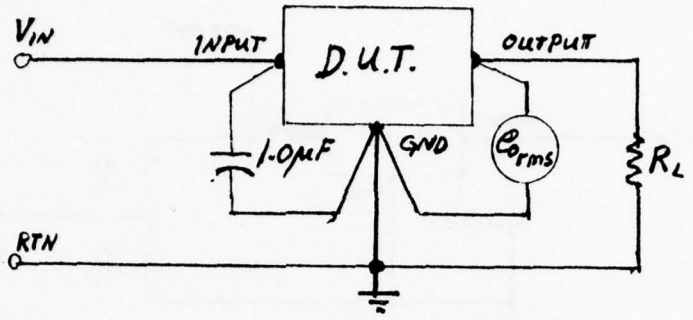


Figure 10-13. Noise test circuit

The Line Transient Response Test Circuit, shown in figure 10-14, is essentially the same as the original version, except that the transient voltage circuit has been added for clarification and the load resistor values have been changed to increase the static load current.

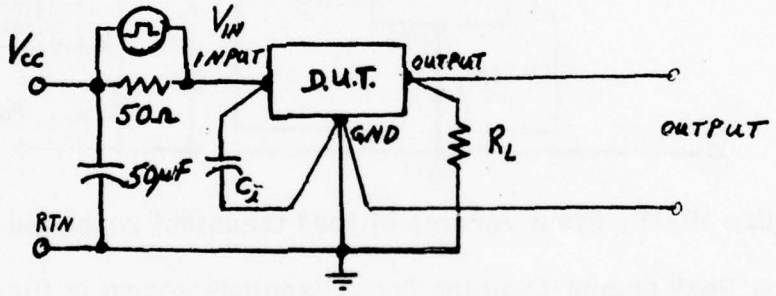


Figure 10-14. Line transient response test circuit

The Load Transient Response Test Circuit is shown in figures 10-15 and 10-16. In the original version, this test is accomplished by injecting a current pulse into the junction of the two load resistors, R_2 and R_3, and measuring the transients at the output of the device under test. However, the current levels used in this test were not typical of the current levels anticipated in typical applications. When the current levels were increased to typify actual applications, the injected current pulses exceeded the capability of available test equipment. Therefore, it was necessary to change the test method for generating the current pulse. The final version of the test circuit is shown in figure 10-16.

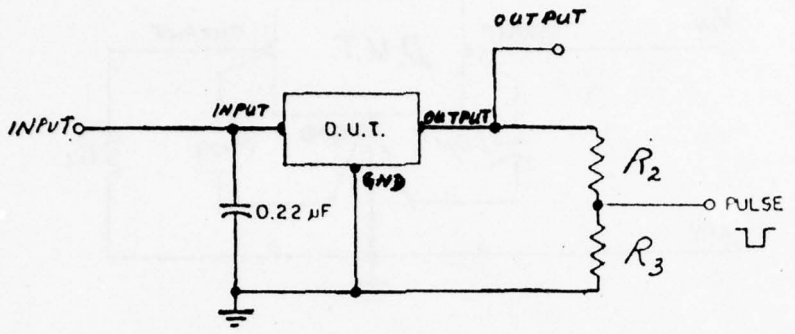


Figure 10-15. Original version of load transient response test circuit

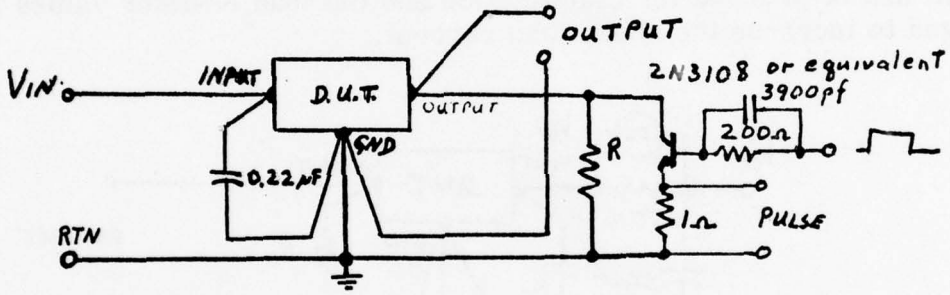


Figure 10-16. Final version of load transient response test circuit

The Peak Output Current Test Circuit is shown in figures 10-17 and 10-18. Figure 10-17 shows the original version of the peak output current test circuit. This circuit was unsatisfactory because: (a), a minimum beta transistor can cause a five percent error in the measurement, (b), in the emitter follower test circuit for the pulse generator, even with no collector current, the emitter is a diode drop lower than the base voltage, and, (c), the output voltage is lowered by the circuit to some uncontrolled level so that the excess (V_{in} - V_{out}) voltage can cause local heating of the device under test and, thus, oscillations of the output current.

The final version of the test circuit provides control of the output voltage. When the pulse is applied to the base of transistor Q3, the transistor saturates. This provides base current for transistors Q1 and Q2. The supply voltage V_X serves to clamp the base of transistor Q2 to the voltage level V_X. Therefore, while the pulse is applied to Q3, the device output is clamped to V_X plus two base-emitter drops. By controlling the output voltage point, excess local heating and, hence, current oscillations are prevented.

Below is shown the effect of the controlled voltage point on the peak output current for a five-volt regulator.

Output current versus forced Δ output voltage

Forced Δ Output Voltage, V	Peak Current, A
.25	1.15
.5	1.15
1.0	1.15
1.5	1.15
2.0	1.20 *

* Current oscillations began when the output voltage was forced to 2.0 volts below the nominal output voltage.

As shown above, a slight increase in the peak output current level occurs as the device begins to current oscillate. Since it is not feasible to perform automatic testing with the device oscillating, it is recommended that the forced output voltage test be used even though the peak output, during the oscillating condition, may be slightly (about five percent) higher.

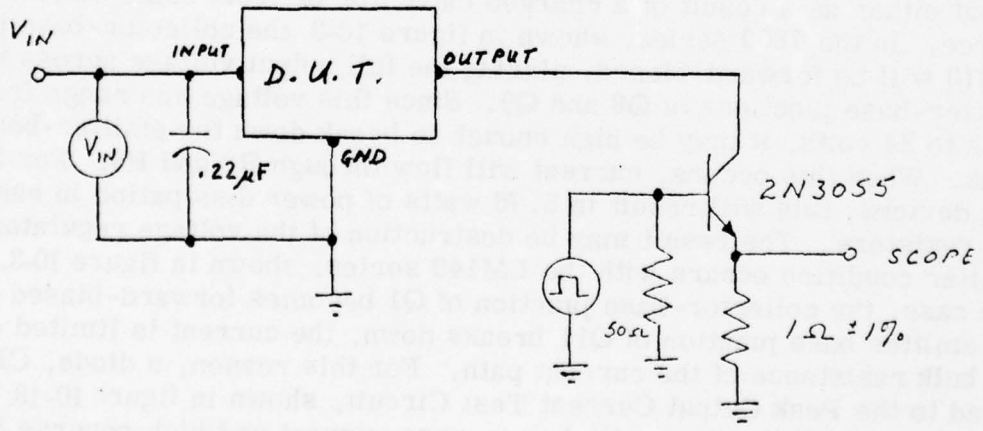


Figure 10-17. Original version of peak output current test circuit

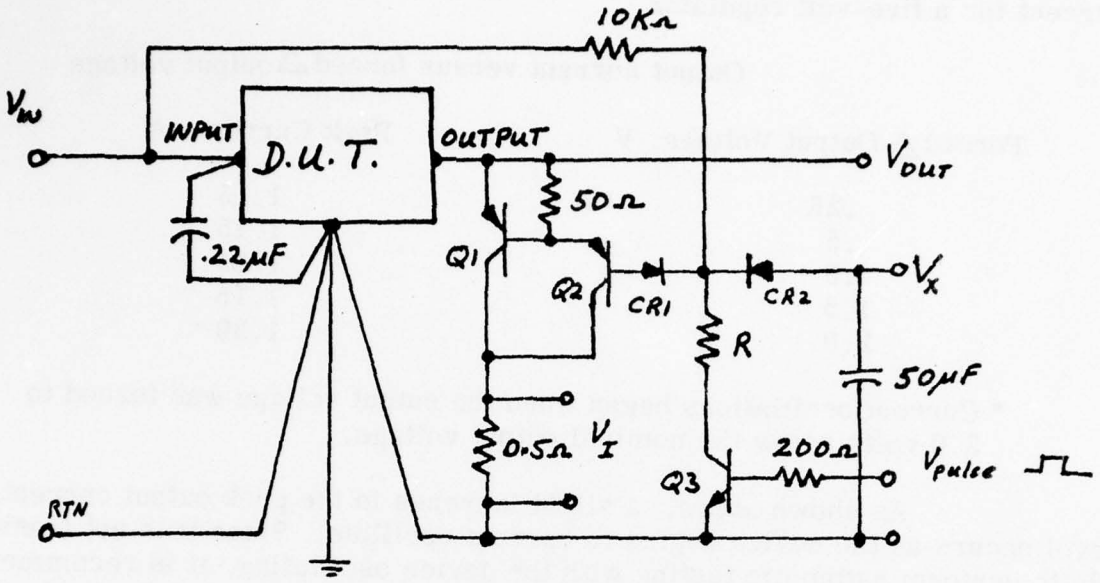


Figure 10-18. Final version of peak output current test circuit

10.6 Discussions of Anomalies

The most apparent irregularity of these voltage regulators is the current oscillation problem discussed in 10.5. Further investigations have disclosed a problem if the regulator is forced to sink current. This can occur when the input voltage is reduced to zero while voltage remains at the output either as a result of a charged capacitor or from some other voltage source. In the 7800 series, shown in figure 10-2 the collector-base junction of Q10 will be forward-biased, placing the full output voltage across the emitter-base junctions of Q8 and Q9. Since this voltage can range from five volts to 24 volts, it may be high enough to break down the emitter-base junctions. When this occurs, current will flow through R8 and R9. For the 24-volt devices, this will result in 5.76 watts of power dissipation in each of the two resistors. The result may be destruction of the voltage regulator. A similar condition occurs with the LM140 series, shown in figure 10-3. In this case, the collector-base junction of Q1 becomes forward-biased and, if the emitter base junction of Q11 breaks down, the current is limited only by the bulk resistance of the current path. For this reason, a diode, CR1, was added to the Peak Output Current Test Circuit, shown in figure 10-18. The diode is a regulating type with low inverse current and high reverse breakdown voltage requirements.

10.7 Recommendations

Anomalies exist in each device and generally limit device performance and operation. Some are readily apparent and can be compensated for by good circuit design. Other anomalies are more subtle and may not immediately be recognized by the design engineer. For these reasons, a section should be added to the slash sheet to list anomalies. Such a section will be of particular benefit to the device user. However, the manufacturer will benefit by being informed of certain design deficiencies in his product.

Table 10-2. Electrical parameter comparison, device type 02 (case x)
($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	7 10 35	-5 -500 -50	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	4.75 4.80 4.75	5.25 5.20 5.25	Volts
Line Regulation	7 to 25	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-25 -20 -25	+25 +20 +25	mV
Load Regulation	10	-500 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-75 -50 -75	+75 +50 +75	mV
Standby Current Drain	7 25 7	-5 -5 -500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	7 to 25	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	7	-500 to -5		-0.5	0	mA
Output Short Circuit Current	10			-0.7	-0.1	A
Peak Output Current	10		$T_A = 25°C$ sample only	-1.0	-0.7	A

Table 10-2. Electrical parameter comparison, device type 02 (case x) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	8 20 35	-5, -500 -5, -500 -5, -50		4.75	5.25	Volts
	10	-5	$T_A = 150°C$	4.70	5.30	
Line Regulation	8 to 35 8 to 25	-50 -350		-150 -50	+150 +50	mV
Load Regulation	10 35	-500 to -5 -50 to -5		-100 -150	+100 +150	mV
Standby Current Drain	10 35	-5 -5		-7.0 -8.0	-0.5 -0.5	mA
Standby Current Drain Change Vs. Line Voltage	8 to 35	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	10	-500 to -5		-0.5	+0.5	mA
Output Short Circuit Current	10 25 35			-2.00 -1.50 -1.00	-0.01 -0.01 -0.01	A
Peak Output Current	8 forced $\Delta V_{out} = 0.48$		100% Test	-2.00	-0.50	A

Table 10-2 (cont'd). Electrical parameter comparison, device type 02 (case x) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	10	-50	ΔV_{in}=1 Vrms BW=10 Hz to 100K Hz	60	--	dB
Output Noise Voltage	10	-50	BW=10 Hz to 100K Hz	--	120	μV_{rms}
Line Transient Response	10	-1	ΔV_{in}=3 V	--	4	m V/V
Load Transient Response	10	-40	ΔI_L=-10 mA		1.0	m V/mA
Average Temperature Coefficient of Output Voltage	7	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-1.25 -1.25	+1.25 +1.25	m V/°C
Startup Input Voltage				--	9	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-2 (cont'd). Electrical parameter comparison, device type 02 (case x)
($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	10 *1	-125	Meter BW 10 Hz to 10K Hz	60	--	dB
Output Noise Voltage	10	-50	$T_A = 25°C$ sample only	--	125	μ Vrms
Line Transient Response	10 **3	-5	$T_A = 25°C$ sample only	--	30	m V/V
Load Transient Response	10	-50 ++-200	$T_A = 25°C$ sample only	--	2.5	m V/m A
Average Temperature Coefficient of Output Voltage	10	-5	sample only	-2.00	+2.00	m V/ °C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* Vripple @ 120 Hz (rms)

** Vpulse

++ ΔI_L

Table 10-3. Electrical parameter comparison, device type 03 (case x) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	14.5 17 35	-5 -500 -50	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	11.40 11.50 11.40	12.60 12.50 12.60	Volts
Line Regulation	14.5 to 35	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-60 -50 -60	+60 +50 +60	mV
Load Regulation	17	-500 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-180 -120 -180	+180 +120 +180	mV
Standby Current Drain	14.5 30 14.5	-5 -5 -500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	14.5 to 30	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	14.5	-500 to -5		-0.5	0	mA
Output Short Circuit Current	17			-0.5	-0.1	A
Peak Output Current	17		$T_A = 25°C$ sample only	-1.0	-0.7	A

Table 10-3. Electrical parameter comparison, device type 03 (case x) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	15 27 35	-5, -500 -5, -500 -5, -50		11.40	12.60	Volts
	17	-5	$T_A = 150°C$	11.28	12.72	
Line Regulation	15 to 35 15 to 32	-50 -350		-360 -120	+360 +120	mV
Load Regulation	17 35	-500 to -5 -50 to -5		-240 -360	+240 +360	mV
Standby Current Drain	17 35	-5 -5		-7.0 -8.0	-0.5 -0.5	mA
Standby Current Drain Change Vs. Line Voltage	15 to 35	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	17	-500 to -5		-0.5	+0.5	mA
Output Short Circuit Current	17 32 35			-1.75 -1.25 -1.00	-0.01 -0.01 -0.01	A
Peak Output Current	15 forced ΔV_{out} = 1.13		100% Test	-2.00	-0.50	A

Table 10-3 (cont'd). Electrical parameter comparison, device type 03 (case x) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	17.5	-50	ΔV_{in}=1Vrms BW=10 Hz to 100K Hz	60	--	dB
Output Noise Voltage	17.5	-50	BW=10 Hz to 100K Hz	--	180	μV_{rms}
Line Transient Response	17.5	-1	ΔV_{in}=3V	--	4.0	mV/V
Load Transient Response	17.5	-40	ΔI_L=-10mA	--	1.0	mV/mA
Average Temperature Coefficient of Output Voltage	14.5	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-3.0 -3.0	+3.0 +3.0	mV/°C
Startup Input Voltage				--	16.5	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-3 (cont'd). Electrical parameter comparison, device type 03 (case x) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	17 *1	-125	Meter BW 10 Hz to 10K Hz	55	--	dB
Output Noise Voltage	17	-50	T_A = 25°C sample only	--	250	μ Vrms
Line Transient Response	17 **3	-5	T_A = 25°C sample only	--	30.0	mV/V
Load Transient Response	17	-50 ++-200	T_A = 25°C sample only	--	2.5	mV/mA
Average Temperature Coefficient of Output Voltage	17	-5		-3.0	+3.0	mV/°C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* V_{ripple} @ 120 Hz (rms)

** V_{pulse}

++ ΔI_L

Table 10-4. Electrical parameter comparison, device type 04 (case x) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	17.5 20 35	-5 -500 -50	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	14.25 14.40 14.25	15.75 15.60 15.75	Volts
Line Regulation	17.5 to 35	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-75 -60 -75	+75 +60 +75	mV
Load Regulation	20	-500 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-225 -150 -225	+225 +150 +225	mV
Standby Current Drain	17.5 30 17.5	-5 -5 -500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	17.5 to 30	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	17.5	-500 to -5		-0.5	0	mA
Output Short Circuit Current	20			-0.5	-0.1	A
Peak Output Current	20		$T_A = 25°C$ sample only	-1.0	-0.7	A

Table 10-4. Electrical parameter comparison, device type 04 (case x) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	18.5 30 35	-5, -500 -5, -500 -5, -50		14.25	15.75	Volts
	20	-5	$T_A = 150°C$	14.10	15.90	
Line Regulation	18.5 to 35	-350		-150	+150	mV
Load Regulation	20	-500 to -5		-300	+300	mV
	35	-50 to -5		-450	+450	
Standby Current Drain	20 35	-5 -5		-7.0 -8.0	-0.5 -0.5	mA
Standby Current Drain Change Vs. Line Voltage	18.5 to 35	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	20	-500 to -5		-0.5	+0.5	mA
Output Short Circuit Current	20 35			-1.75 -1.00	-0.01 -0.01	A
Peak Output Current	18.5 forced ΔV_{out} = 1.43		100% Test	-2.00	-0.50	A

Table 10-4 (cont'd). Electrical parameter comparison, device type 04 (case x) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	20.5	-50	$\Delta V_{in} = 1 V_{rms}$ BW = 10 Hz to 100K Hz	60	--	dB
Ouput Noise Voltage	20.5	-50	BW = 10 Hz to 100K Hz	--	180	μV_{rms}
Line Transient Response	20.5	-1	$\Delta V_{in} = 3$ V	--	4.0	mV/V
Load Transient Response	20.5	-40	$\Delta I_L = -10$ mA	--	1.0	mV/mA
Average Temperature Coefficient of Output Voltage	17.5	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-3.75 -3.75	+3.75 +3.75	mV/°C
Startup Input Voltage				--	19.5	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-4(cont'd). Electrical parameter comparison, device type 04 (case x)
($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	20 *1	-125	Meter BW 10 Hz to 10K Hz	53	--	dB
Output Noise Voltage	20	-50	T_A = 25°C sample only	--	300	μV_{rms}
Line Transient Response	20 **3	-5	T_A = 25°C sample only	--	30.0	mV/V
Load Transient Response	20	-50 ++-200	T_A = 25°C sample only	--	2.5	mV/mA
Average Temperature Coefficient of Output Voltage	20	-5		-3.75	+3.75	mV/°C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* V_{ripple} @ 120 Hz (rms)

** Vpulse

++ ΔI_L

Table 10-5. Electrical parameter comparison, device type 05 (case x) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	27 40 29 40	-5 -5 -500 -75	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	23.00 23.30 23.00	25.00 24.70 25.00	Volts
Line Regulation	27 to 40	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-120 -100 -120	+120 +100 +120	mV
Load Regulation	29	-500 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-240 -180 -240	+240 +180 +240	mV
Standby Current Drain	27 40 27	-5 -5 -500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	27 to 40	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	27	-500 to -5		-0.5	0	mA
Output Short Circuit Current	29			-0.3	-0.1	A
Peak Output Current	29		$T_A = 25°C$ sample only	-1.0	-0.7	A

Table 10-5. Electrical parameter comparison, device type 05 (case x) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	28 38 40	-5, -500 -5, -500 -5, -50		22.80	25.20	Volts
	30	-5	$T_A = 150°C$	22.56	25.44	
Line Regulation	28 to 40 28 to 38	-50 -350		-720 -240	+720 +240	mV
Load Regulation	30 40	-500 to -5 -50 to -5		-480 -720	+480 +720	mV
Standby Current Drain	30 40	-5 -5		-7.0 -8.0	-0.5 -0.5	mA
Standby Current Drain Change Vs. Line Voltage	28 to 40	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	30	-500 to -5		-0.5	+0.5	mA
Output Short Circuit Current	30 38 40			-1.25 -1.00 -1.00	-0.01 -0.01 -0.01	A
Peak Output Current	28 forced ΔV_{out} = 2.28		100% Test	-2.00	-0.50	A

Table 10-5 (cont'd). Electrical parameter comparison, device type 05 (case x) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	30	-50	$\Delta V_{in} = 1V_{rms}$ BW = 10 Hz to 100K Hz	60	--	dB
Output Noise Voltage	30	-50	BW = 10 Hz to 100K Hz	--	240	μV_{rms}
Line Transient Response	30	-1	$\Delta V_{in} = 3V$	--	4.0	mV/V
Load Transient Response	30	-40	$\Delta I_L = -10mA$	--	1.0	mV/mA
Average Temperature Coefficient of Output Voltage	27	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-6.0 -6.0	+6.0 +6.0	mV/°C
Startup Input Voltage				--	29.0	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-5(cont'd). Electrical parameter comparison, device type 05 (case x) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	30 *1	-125	Meter BW 10 Hz to 10K Hz	50	--	dB
Output Noise Voltage	30	-50	T_A = 25°C sample only	--	500	μV_{rms}
Line Transient Response	30 **3	-5	T_A = 25°C sample only	--	30.0	mV/V
Load Transient Response	30	-50 ++-200	T_A = 25°C sample only	--	2.5	mV/mA
Average Temperature Coefficient of Output Voltage	30	-5	sample only	-6.0	+6.0	mV/°C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* V_{ripple} @ 120 Hz (rms)

** V_{pulse}

++ ΔI_L

Table 10-6. Electrical parameter comparison, device type 06 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	7 10 20 35	-5 -1,500 -750 -200	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	4.75 4.80 4.75	5.25 5.20 5.25	Volts
Line Regulation	7 to 25	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-25 -20 -25	+25 +20 +25	mV
Load Regulation	10 20	-1,500 to -5 750 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-75 -50 -75	+75 +50 +75	mV
Standby Current Drain	7 25 7	-5 -5 -1,500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	7 to 25	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	7	-1,500 to -5		-0.5	0	mA
Output Short Circuit Current	10			-2.0	-0.3	A
Peak Output Current	10		$T_A = 25°C$ sample only	-3.0	-2.0	A

Table 10-6. Electrical parameter comparison, device type 06 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)						
Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	8 20 35	-5, -1,000 -5, -1,000 -5, -100		4.75	5.25	Volts
	10	-5	T_A - 150°C	4.70	5.30	
Line Regulation	8 to 35 8 to 25	-100 -500		-150 -50	+150 +50	mV
Load Regulation	10 35	-1,000 to -5 -100 to -5		-100 -150	+100 +150	mV
Standby Current Drain	10 35	-5 -5		-7.0 -8.0	-0.5 -0.5	mA
Standby Current Drain Change Vs. Line Voltage	8 to 35	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	10	-1,000 to -5		-0.5	+0.5	mA
Output Short Circuit Current	10 25 35			-4.0 -3.0 -2.0	-0.02 -0.02 -0.02	A
Peak Output Current	8 forced ΔVout = 0.48		100% Test	-4.0	-1.0	A

Table 10-6 (cont'd). Electrical parameter comparison, device type 06 (case y) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	10	-200	ΔV_{in}=1Vrms BW = 10 Hz to 100K Hz	60	--	dB
Output Noise Voltage	10	-200	BW = 10 Hz to 100K Hz	--	120	μV_{rms}
Line Transient Response	10	-1	ΔV_{in} = 3V	--	4.0	mV/V
Load Transient Response	10	-40	ΔI_L=-10mA	--	1.0	mV/mA
Average Temperature Coefficient of Output Voltage	7	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-1.25 -1.25	+1.25 +1.25	mV/°C
Startup Input Voltage				--	9	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-6 (cont'd). Electrical parameter comparison, device type 06 (case y) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	10 *1	-350	Meter BW 10 Hz to 10K Hz	60	--	dB
Output Noise Voltage	10	-100	T_A = 25°C sample only	--	125	μV_{rms}
Line Transient Response	10 **3	-5	T_A = 25°C sample only	--	30	mV/V
Load Transient Response	10	-100 ++-400	T_A = 25°C sample only	--	2.5	mV/mA
Average Temperature Coefficient of Output Voltage	10	-5	sample only	-2.0	+2.0	mV/°C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* Vripple @ 120 Hz (rms)

** Vpulse

++ΔI_L

Table 10-7. Electrical parameter comparison, device type 07 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	14.5 17 30 35	-5 -1,500 -750 -200	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	11.40 11.50 11.40	12.60 12.50 12.60	Volts
Line Regulation	14.5 to 35	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-60 -50 -60	+60 +50 +60	mV
Load Regulation	17 30	-1,500 to -5 -750 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-180 -120 -180	+180 +120 +180	mV
Standby Current Drain	14.5 30 14.5	-5 -5 -1,500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	14.5 to 30	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	14.5	-1,500 to -5		-0.5	0	mA
Output Short Circuit Current	17			-1.0	-0.15	A
Peak Output Current	17		$T_A = 25°C$ sample only	-3.0	-2.0	A

Table 10-7. Electrical parameter comparison, device type 07 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	15 27 35	-5, -1,000 -5, -1,000 -5, -100		11.40	12.60	Volts
	17	-5	$T_A = 150°C$	11.28	12.72	
Line Regulation	15 to 35 15 to 32	-100 -500		-360 -120	+360 +120	mV
Load Regulation	17 35	-1,000 to -5 -100 to -5		-240 -360	+240 +360	mV
Standby Current Drain	17 35	-5 -5		-7.0 -8.0	-.5 -.5	mA
Standby Current Drain Change Vs. Line Voltage	15 to 35	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	10	-1,000 to -5		-0.5	+0.5	mA
Output Short Circuit Current	17 32 35			-3.5 -2.5 -2.00	-0.02 -0.02 -0.02	A
Peak Output Current	8 forced ΔV_{out} = 1.13		100% Test	-4.0	-1.0	A

Table 10-7(cont'd). Electrical parameter comparison, device type 07 (case y) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	17.5	-200	ΔV_{in}=1Vrms BW = 10 Hz to 100K Hz	60	--	dB
Output Noise Voltage	17.5	-200	BW = 10 Hz to 100K Hz	--	180	μ Vrms
Line Transient Response	17.5	-1	ΔV_{in} = 3V	--	4.0	mV/V
Load Transient Response	17.5	-40	ΔI_L = 10mA	--	1.0	mV/mA
Average Temperature Coefficient of Output Voltage	14.5	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-3.0 -3.0	+3.0 +3.0	mV/°C
Startup Input Voltage				--	16.5	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-7(cont'd). Electrical parameter comparison, device type 07 (case y)
($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	17 *1	-350	Meter BW 10Hz to 10K Hz	55		dB
Output Noise Voltage	17	-100	$T_A = 25°C$ sample only	--	250	μV_{rms}
Line Transient Response	17 **3	-5	$T_A = 25°C$ sample only	--	30.0	mV/V
Load Transient Response	17	-100 ++ -400	$T_A = 25°C$ sample only	--	2.5	mV/mA
Average Temperature Coefficient of Output Voltage	17	-5		-3.0	+3.0	mV/°C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* V_{ripple} @ 120 Hz (rms)

** V_{pulse}

++ ΔI_L

Table 10-8. Electrical parameter comparison, device type 08 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	17.5 20 30 35	-5 -1,500 -750 -200	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	14.25 14.40 14.25	15.75 15.60 15.75	Volts
Line Regulation	17.5 to 35	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-75 -60 -75	+75 +60 +75	mV
Load Regulation	20 30	-1,500 to -5 -750 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-225 -150 -225	+225 +150 +225	mV
Standby Current Drain	17.5 30 17.5	-5 -5 -1,500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	17.5 to 30	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	17.5	-1,500 to -5		-0.5	0	mA
Output Short Circuit Current	20			-1.0	-0.15	A
Peak Output Current	20		$T_A = 25°C$ sample only	-3.0	-2.0	A

Table 10-8. Electrical parameter comparison, device type 08 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	18.5 30 35	-5, -1,000 -5, -1,000 -5, -100		14.25	15.75	Volts
	20	-5	$T_A = 150°C$	14.10	15.90	
Line Regulation	18.5 to 35	-500		-150	+150	mV
Load Regulation	20 35	-1,000 to -5 -100 to -5		-300 -450	+300 +450	mV
Standby Current Drain	20 35	-5 -5		-7.0 -8.0	-0.5 -0.5	mA
Standby Current Drain Change Vs. Line Voltage	18.5 to 35	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	20	-1,000 to -5		-0.5	+0.5	mA
Output Short Circuit Current	20 35			-3.5 -2.0	-0.02 -0.02	A
Peak Output Current	18.5 forced ΔV_{out} = 1.43			-4.0	-1.0	A

Table 10-8(cont'd). Electrical parameter comparison, device type 08 (case y) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	20.5	-200	ΔV_{in} = 1 V_{rms} BW = 10 Hz to 100K Hz	60	--	dB
Output Noise Voltage	20.5	-200	BW = 10 Hz to 100K Hz	--	180	μ Vrms
Line Transient Response	20.5	-1	ΔV_{in} = 3V	--	4.0	mV/V
Load Transient Response	20.5	-40	ΔI_L = -10mA	--	1.0	mV/mA
Average Temperature Coefficient of Output Voltage	17.5	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-3.75 -3.75	+3.75 +3.75	mV/°C
Startup Input Voltage				--	19.5	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-8 (cont'd). Electrical parameter comparison, device type 08 (case y) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	20 *1	-350	Meter BW 10 Hz to 10K Hz	53	--	dB
Output Noise Voltage	20	-100	$T_A = 25°C$ sample only	--	300	μV_{rms}
Line Transient Response	20 **3	-5	$T_A = 25°C$ sample only	--	30	mV/V
Load Transient Response	20	-100 ++-400	$T_A = 25°C$ sample only		2.5	mV/mA
Average Temperature Coefficient of Output Voltage	20	-5		-3.75	+3.75	mV/°C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* V_{ripple} @ 120 Hz (rms)

** V_{pulse}

++ ΔI_L

Table 10-9. Electrical parameter comparison, device type 09 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	27 40 29 40	-5 -5 -1,500 -750	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	23.00 23.30 23.00	25.00 24.70 25.00	Volts
Line Regulation	27 to 40	-5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-120 -100 -120	+120 +100 +120	mV
Load Regulation	29 40	-1,500 to -5 -750 to -5	$T_A = -55°C$ $T_A = 25°C$ $T_A = 125°C$	-240 -180 -240	+240 +180 +240	mV
Standby Current Drain	27 40 27	-5 -5 -1,500		-10	0	mA
Standby Current Drain Change Vs. Line Voltage	27 to 40	-5		-0.8	0	mA
Standby Current Drain Change Vs. Load Current	27	-1,500 to -5		-0.5	0	mA
Output Short Circuit Current	29			-0.5	-0.1	A
Peak Output Current	29		$T_A = 25°C$ sample only	-3.0	-2.0	A

Table 10-9. Electrical parameter comparison, device type 09 (case y) ($-55°C \leq T_A \leq 125°C$ unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Output Voltage	28 38 40	-5, -1,000 -5, -1,000 -5, -100		22.80	25.20	Volts
	30	-5	$T_A = 150°C$	22.56	25.44	
Line Regulation	28 to 40 28 to 38	-100 -500		-720 -240	+720 +240	mV
Load Regulation	30 40	-1,000 to -5 -100 to -5		-480 -720	+480 +720	mV
Standby Current Drain	30 40	-5 -5		-7.0 -8.0	-0.5 -0.5	mA
Standby Current Drain Change Vs. Line Voltage	28 to 40	-5		-1.0	+1.0	mA
Standby Current Drain Change Vs. Load Current	30	-1,000 to -5		-0.5	+0.5	mA
Output Short Circuit Current	30 38 40			-2.5 -2.0 -2.0	-0.02 -0.02 -0.02	A
Peak Output Current	28 forced $\Delta V_{out} = 2.28$			-4.0	-1.0	A

Table 10-9 (cont'd). Electrical parameter comparison, device type 09 (case y) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Original Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	30	-200	$\Delta V_{in} = 1 V_{rms}$ BW = 10 Hz to 100K Hz	60	--	dB
Output Noise Voltage	30	-200	BW=10 Hz to 100K Hz	--	240	μV_{rms}
Line Transient Response	30	-1	$\Delta V_{in} = 3V$	--	4.0	mV/V
Load Transient Response	30	-40	$\Delta I_L = -10mA$	--	1.0	mV/mA
Average Temperature Coefficient of Output Voltage	27	-5	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-6.0 -6.0	+6.0 +6.0	mV/°C
Startup Input Voltage				--	29.0	Volts
Thermal Shutdown Point			sample only	165	185	°C

Table 10-9(cont'd). Electrical parameter comparison, device type 09 (case y) ($-55°C \leq T_A \leq 125°C$, unless otherwise stated)

Characteristics	Final Recommendations					Units
	Conditions			Limits		
	V, Input Voltage	mA, Load Current	Other	Min	Max	
Ripple Rejection	30 *1	-350	Meter BW 10 Hz to 10K Hz	50	--	dB
Output Noise Voltage	30	-100	$T_A = 25°C$ sample only	--	500	μ Vrms
Line Transient Response	30 **3	-5	$T_A = 25°C$ sample only	--	30	mV/V
Load Transient Response	30	-100 ++-400	$T_A = 25°C$ sample only	--	2.5	mV/mA
Average Temperature Coefficient of Output Voltage	30	-5	sample only	-6.0	+6.0	mV/°C
Startup Input Voltage	Deleted					Volts
Thermal Shutdown Point	P/O Burn-in					°C

* V_{ripple} @ 120 Hz (rms)

** V_{pulse}

++ ΔI_L

SECTION XI

MIL-M-38510/109 PRECISION TIMERS

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SECTION XI

MIL-M-38510/109 PRECISION TIMERS

11.1 Introduction

The specified task with MIL-M-38510/109 was to review and evaluate comments from manufacturers of 555 and 556 timers and markup the preliminary draft. All interested device manufacturers had reviewed and commented on the preliminary draft. The over-all goal was to issue a final slash sheet to assure availability of quality parts at a reasonable price for military users.

11.2 Background

The main problem encountered with accomplishing the stated task was that nearly every manufacturer did not really know his device well enough to respond to the proposed slash sheet. These manufacturers were also hesitant to spend the time and money to determine the problem areas. However, one manufacturer did indicate a great deal of interest and spent the time and money to determine his yield. Three manufacturers had indicated at least mild interest by commenting on the preliminary draft. Their devices were used, as required, to assess potential test/device problems.

The three main manufacturers were Signetics, Motorola and Fairchild. The National device did not conform to the device truth table of all other manufacturers' devices and therefore was dropped from the slash sheet.

11.3 Device Description

11.3.1 Block Diagram

The 555 timer block diagram is shown in figure 11-1. It consists of two voltage comparators, a flip-flop, an output stage, a discharge transistor and a resistive divider. The resistive divider provides reference voltages of 1/3 V_{cc} and 2/3 V_{cc} for the comparators. The threshold comparator uses the 2/3 V_{cc} reference and the trigger comparator uses the 1/3 V_{cc} reference. When the trigger comparator input is less than 1/3 V_{cc} it sets the flip-flop and the output goes to a logic "1" state. The flip-flop is latched to the set state until the threshold comparator input is greater than 2/3 V_{cc}, at which point it resets the flip-flop and the output goes to a logic "0" state. The flip-flop is then latched to the reset state. The flip-flop can also be reset by a logic "0" at its reset input. Figure 11-2 shows the truth table which describes the device's response to the various combinations. A reset signal on the RESET line overrides the set signal on the TRIGGER line (see states 3 and 11 in figure 11-2). However, a reset signal on the THRESHOLD line does not override the set signal on the TRIGGER line (see states 6 and 10 in figure 11-2). The discharge transistor is off when the output is high (set) and on when the output is low (reset).

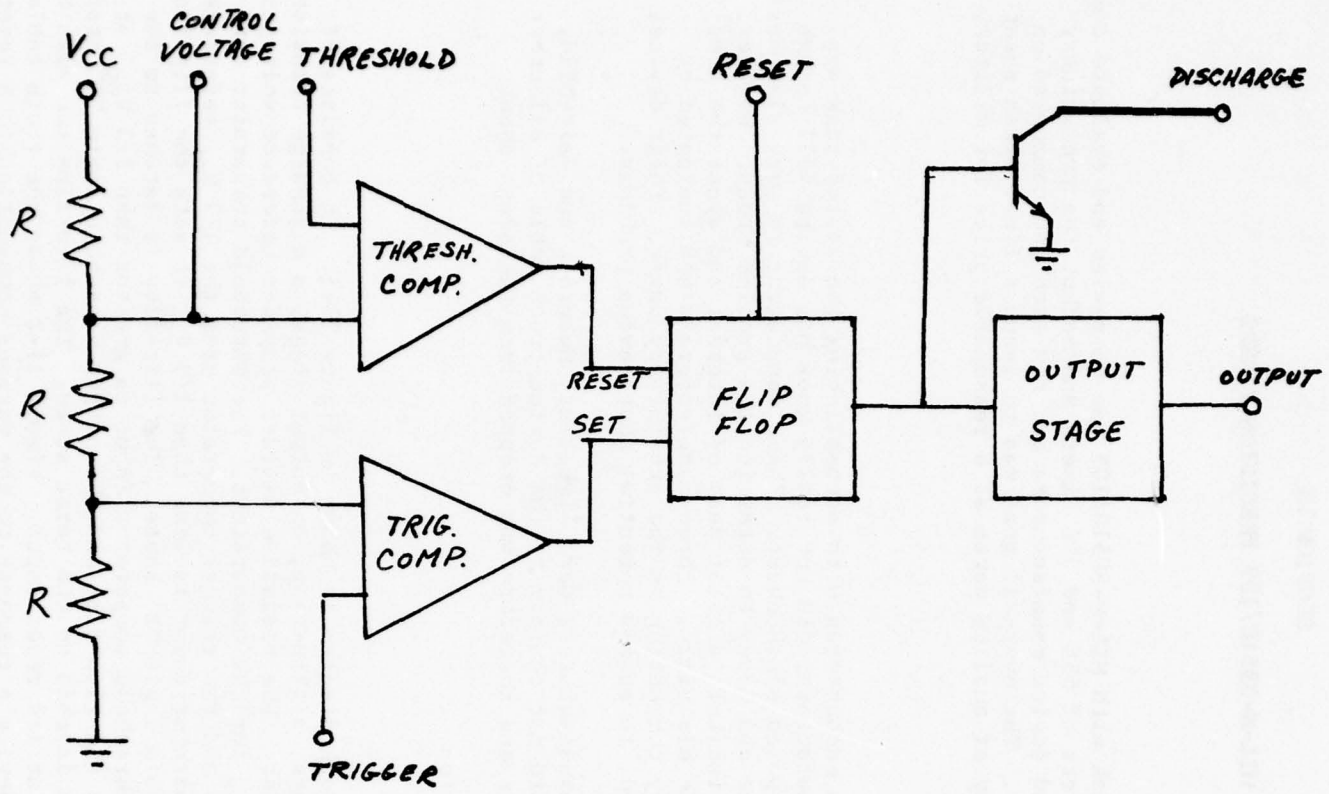


Figure 11-1. Block diagram

INPUTS			OUTPUT
$\overline{\text{RESET}}$	THRESHOLD	$\overline{\text{TRIGGER}}$	
⊔	0	1	RESETS (⊔)
⊔	1	1	0
⊔	0	0	⊔
⊔	1	0	⊔
1	⊓	1	RESETS
1	⊓	0	1
0	⊓	1	0
0	⊓	0	0
1	0	⊔	SETS (⊓)
1	1	⊔	⊓⊔ (SEE NOTE 1)
0	0	⊔	0
0	1	⊔	0

Notes:

1. Some devices latch high for V_{cc} < 10VDC

2. Discharge transistor follows the output as follows:

   Output High = Discharge transistor Off
   Output Low = Discharge transistor ON

Figure 11-2. Device truth table

11.3.2 Circuit Schematic

Referring to figure 11-3, the timer circuit consists of two comparators. The threshold comparator is made up of Q1-Q8 with the output of the comparator at the collector of Q6. When the base of Q1 is at a higher voltage than the base of Q4, Q6 increases its level of conduction from its collector down through Q15 or Q16 (depending on the base drive of Q15). The trigger comparator is made up of Q10-Q13 with the output at the collector of Q11. When the base of Q10 is at a lower voltage than the base of Q13, Q11 will conduct and provide base drive to Q15.

The flip-flop is made up of Q15-Q19 with the output at the collector of Q17 which controls the base of Q20 (in the output stage). The flip-flop is set by turning on Q15 which forces Q16 off and Q17 on. Q20 will then go off and make the output go high. Even when Q15 goes off, Q17 will stay on because Q16 does not have base drive. The flip-flop is reset when Q6 increases its conduction level and turns on Q16 which forces Q17 off. Q20 will then go on and make the output go low. When Q6 decreases its conduction, Q16 gets its base drive through R11 because the base of Q20 will be more than two diode drops above ground and, therefore, force current to flow through R11. When Q15 is turned on to set the flip-flop, the current coming through R11 is diverted from the base of Q16 to Q15, and Q17 goes on as described earlier.

The output stage is made up of Q20-Q24. Q20 controls the output stage. When Q20 is off, Q21 and Q22 are on and can supply current to the load, while Q24 is off. When Q20 is turned on, it turns Q21 and Q22 off and turns Q24 on. Q24 sinks load current. When excessive sink current is required, Q24 comes out of saturation and its collector voltage will rise until Q23 conducts the extra current into Q20 and to ground through several paths (R15, base of Q24 and base of Q14).

The discharge transistor is Q24 which is turned on when Q20 is on and turned off when Q20 is off. When Q23 conducts to help sink load current, that current provides additional base drive for the discharge transistor.

11.3.3 Monostable Operation

In the monostable mode, an external capacitor is charged through an external resistor (connected to V_{cc}) and discharged through the discharge transistor. The THRESHOLD line monitors the capacitor voltage and turns on the discharge transistor when the capacitor voltage gets up to 2/3 V_{cc}. The discharge transistor stays on until a set signal on the TRIGGER line (TRIGGER voltage less than 1/3 V_{cc}) turns the discharge transistor OFF and allows the capacitor to charge up again. Figure 11-4 shows the schematic for monostable operation. A .01 μF capacitor is recommended at CONTROL VOLTAGE pin (2/3 V_{cc} point of resistive divider) to shunt high frequency noise currents to ground. The RESET line should also be connected to V_{cc} to minimize noise pick-up problems.

SCHEMATIC 555 OR 1/2 556 DUAL TIMER

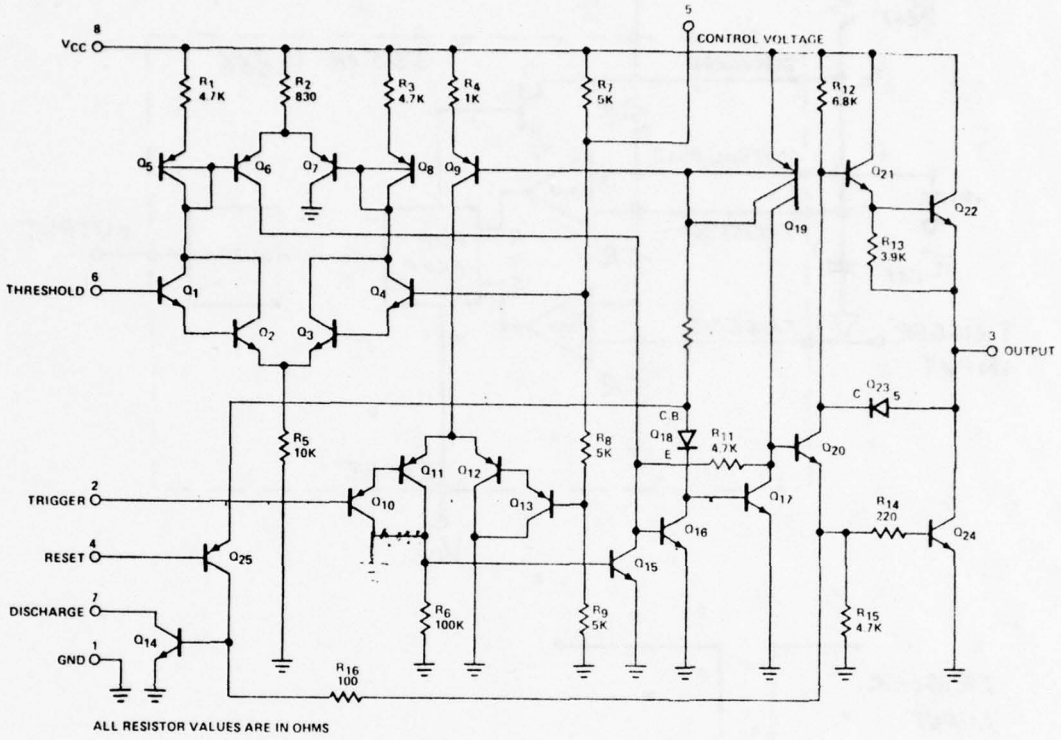


Figure 11-3. Schematic of 555

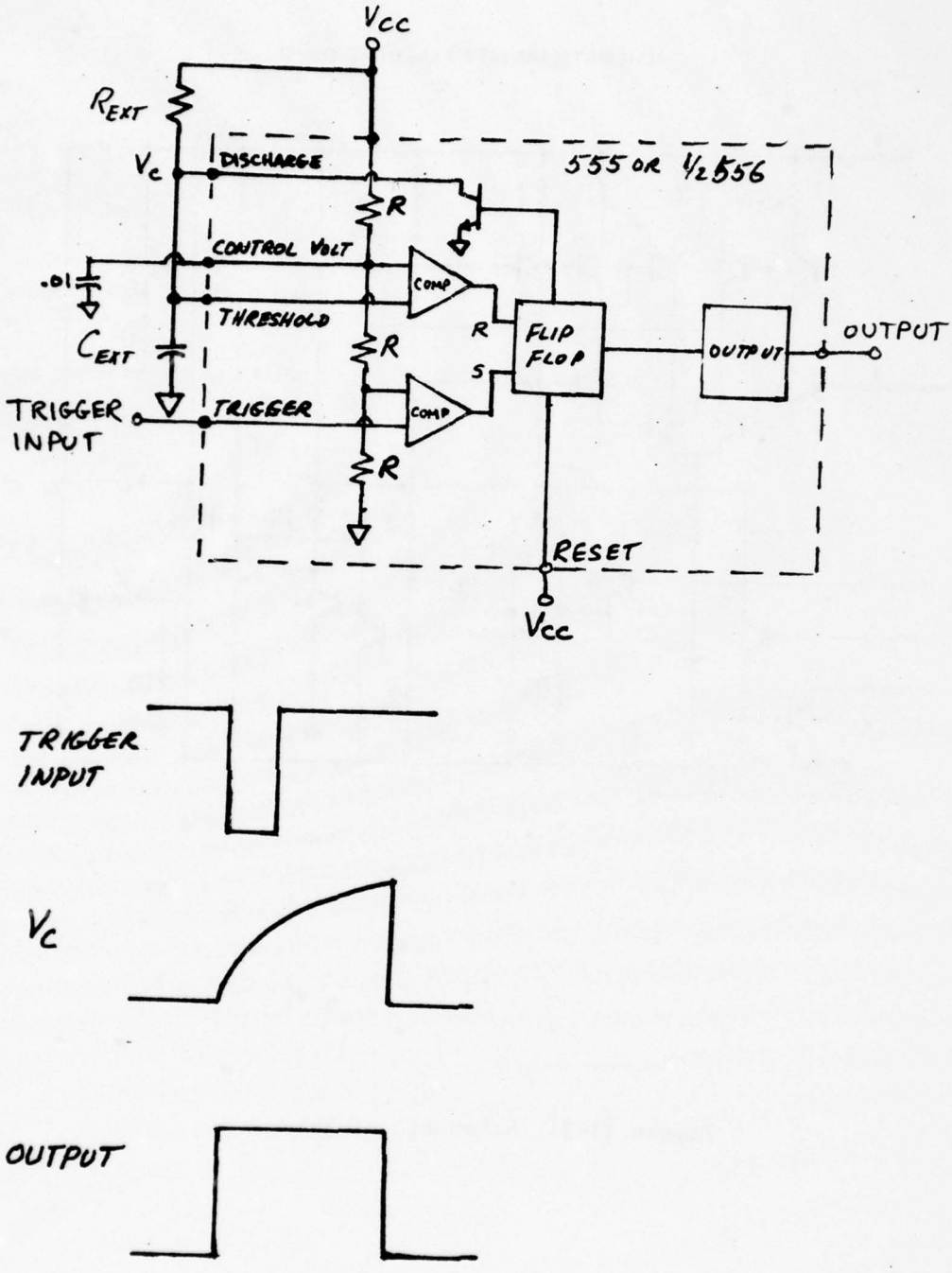


Figure 11-4. Monostable operation

11.3.4 Astable Operation

In the astable mode, a capacitor is charged through two series resistors and discharged through one resistor via the discharge transistor. The THRESHOLD and TRIGGER lines monitor the capacitor voltage and turn the discharge transistor on and off. Figure 11-5 shows the schematic for astable operation. With the discharge transistor off, the capacitor charges up toward V_{cc}. When the voltage gets 2/3 V_{cc}, the THRESHOLD input resets the flip-flop, turning on the discharge transistor. The capacitor discharges toward zero until it reaches 1/3 V_{cc}. The TRIGGER input then sets the flip-flop which turns the discharge transistor off again, and the cycle repeats itself. The voltage waveforms of the capacitor voltage and output are shown in figure 11-5.

11.3.5 Device Idiosyncracies

The 555 timer was originally designed to satisfy the need for a low-cost, commercial timing circuit. Thus, a device with inconsistencies at the output, no T^2L compatibility of reset input over the military temperature range, and lack of accuracy at the military temperatures came into being to meet the needs of the commercial market.

11.3.5.1 Output Waveform Idiosyncrasies

The output waveform has five basic idiosyncrasies. First, a change of slope in the rising edge occurs at approximately three volts with V_{cc} at 4.5 VDC or about 1.5 volts below V_{cc}. Figure 11-6 shows the variation in rising edge between the three manufacturers observed. The sequential turn-on of the two pull-up transistors (Q21 then Q22) is the apparent cause.

Second, a discontinuity in the falling edge of the output waveform, which can cause double triggering of a clock input. The high-to-low transitions for the three manufacturers' devices are shown in figure 11-7. The load dependence of this discontinuity is shown in figure 11-8. The higher the sink current, the longer the time to reach the logic "0" level and the more pronounced the discontinuity appears. The discontinuity occurs about one volt above the logic "0" level. The apparent cause of this discontinuity is that Q20 turns on which turns off the pull-up transistors, so that Q21 and Q22 are off while Q24 is still off. Therefore, the output is pulled low through Q23 so that the output voltage is approximately one volt. When Q24 goes into saturation, the output voltage drops to the V_{sat} of Q24. The higher the sinking current, the longer it takes the base current to saturate Q24, which explains the "tail off" variation observed in figure 11-8. The slight rise in voltage at the one volt level is probably caused by this process: as the load current increases through Q23, its forward voltage increases. Then, as Q24 starts to turn on, load current gets diverted from Q23 into Q24.

Third, a step voltage change at the logic "0" level has been observed as shown in figure 11-9. The variation between manufacturers was quite

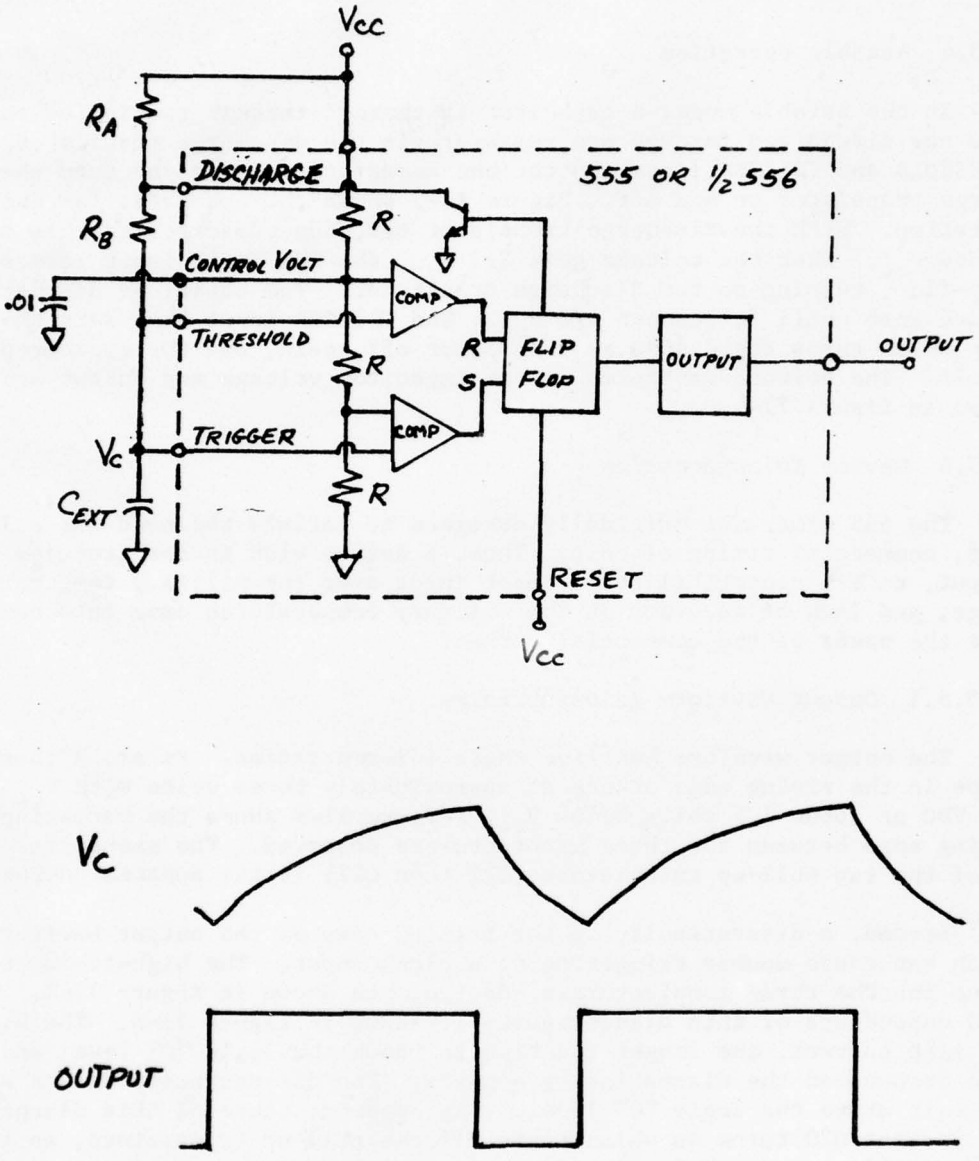
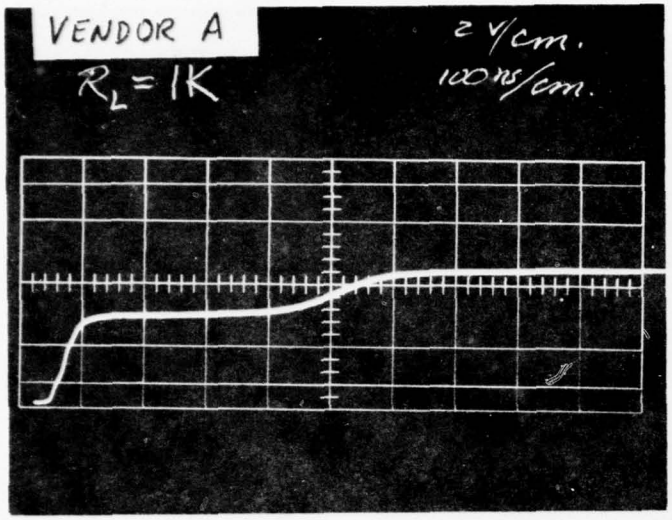
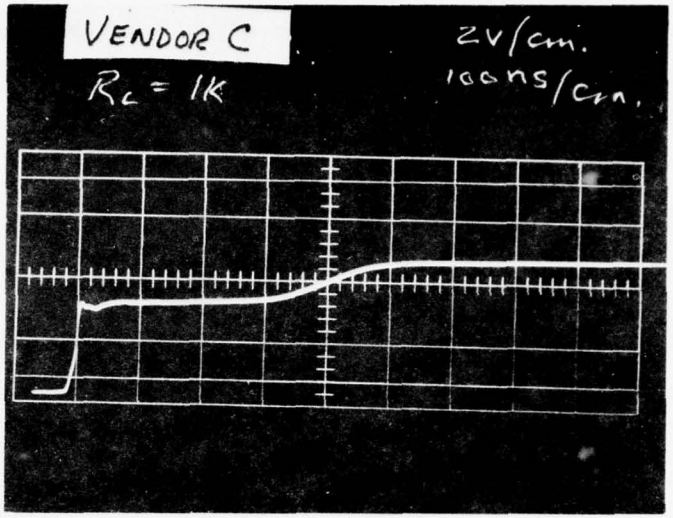
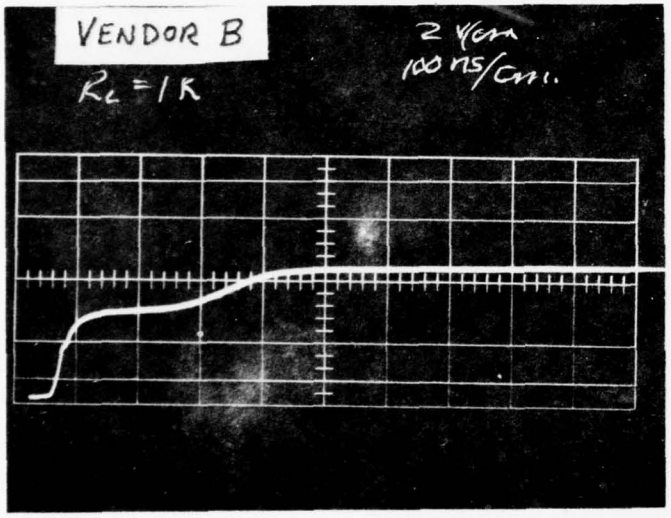


Figure 11-5. Astable operation







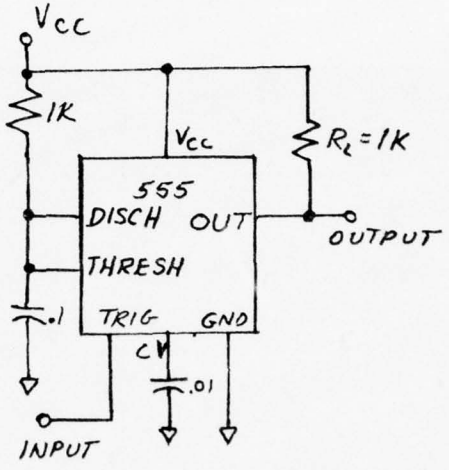
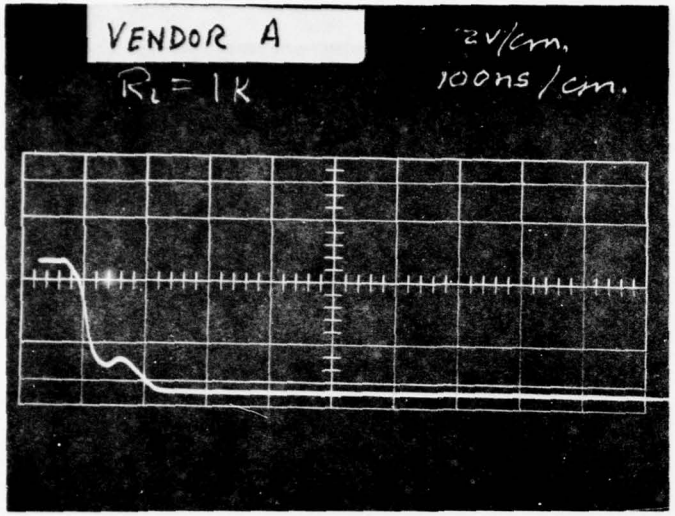
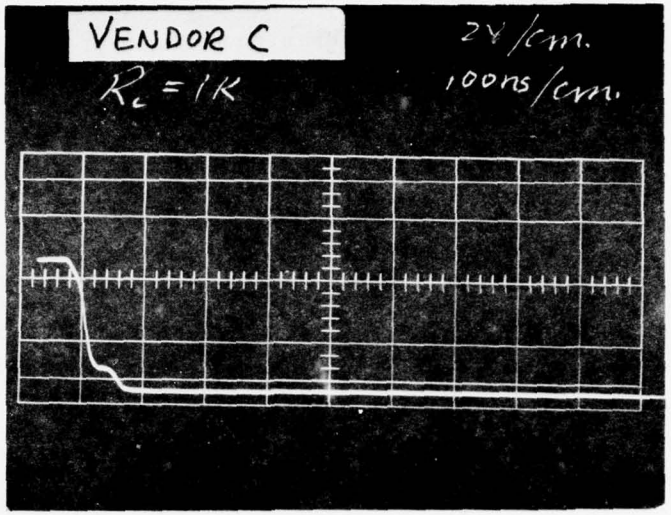
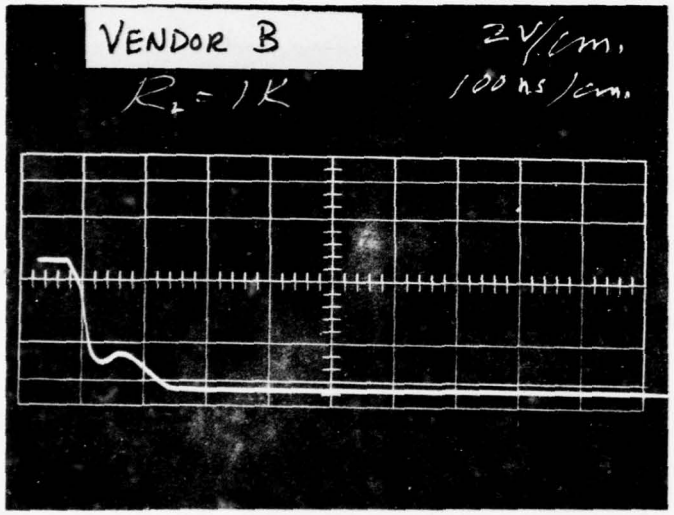


Figure 11-6. Low to high transition at output







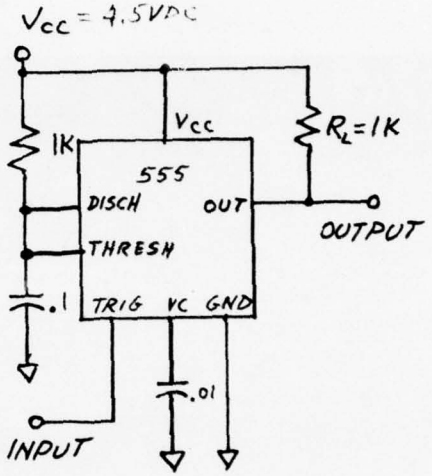
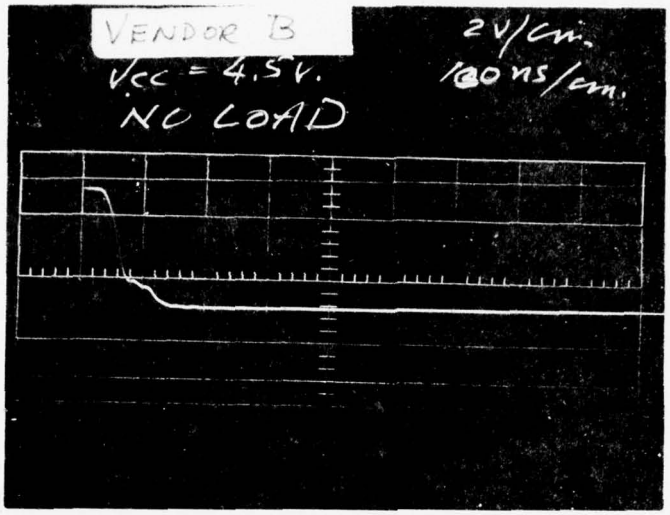
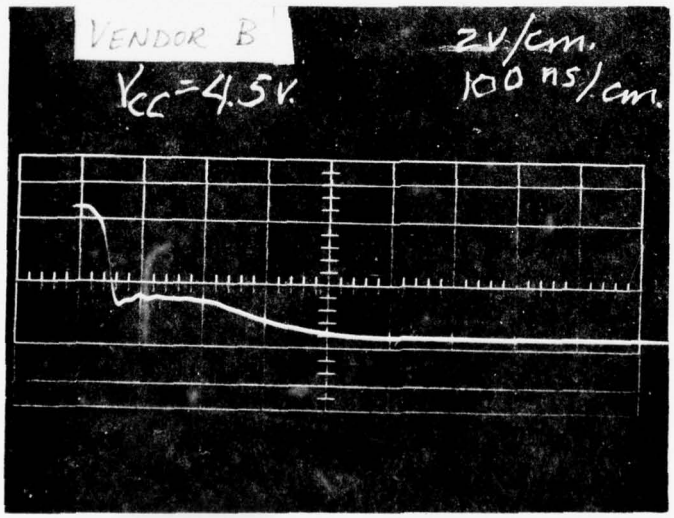


Figure 11-7. High to low transition at output

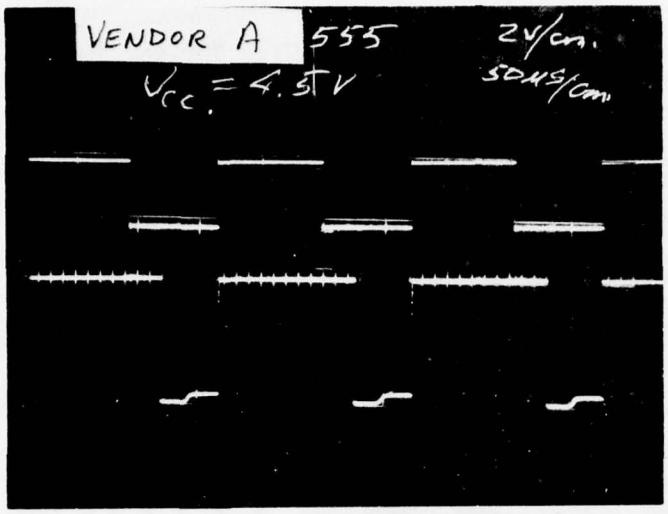


With 300 ohm pull-up resistor



Without 300 ohm pull-up resistor

Figure 11-8. Change in high-to-low transition at output due to loading



Monostable Mode

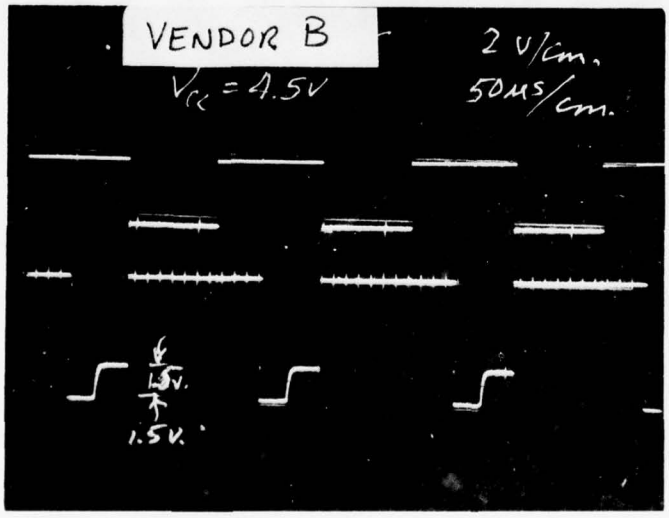
R_L = 300 Ω

V_{cc} = 4.5 V dc

Input

Output

These photos show output logic "0" level change.



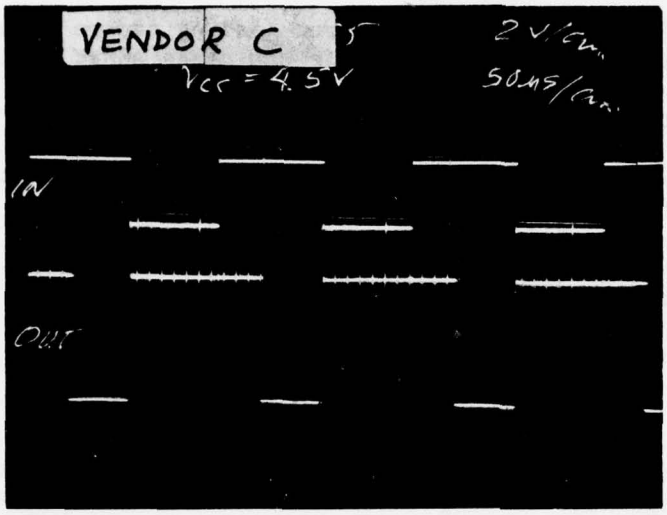
R_L = 300Ω

V_{cc} = 4.5 V dc

Input

Output

Figure 11-9. Variation with vendor of Logic "0" step in monostable mode



R_L = 300 Ω

V_{cc} = 4.5 Vdc

Input

Output

Figure 11-9 (cont'd). Variation with vendor of logic "0" step in monostable mode

dramatic with 300-ohm loading. At the lighter loads, the size of the voltage step becomes reduced significantly. The exact cause of this phenomenon could not be deduced, and the manufacturers were no help. Figure 11-10 shows the disappearance of the voltage step with no pull-up load resistor.

Fourth, a dependence of discharge time on output loading can be seen in figure 11-11 for one manufacturer's device. This can cause additional timing errors if the output load is varying or if the pulse width is set with one load value and used with another load value.

Fifth, if the RESET input is moved slowly through its reset threshold level, the upper and lower totem pole transistors may be on at the same time, causing excessive power dissipation and possible device failure. This is why the RESET input is not tested with a slowly changing voltage ramp. This seems to occur mostly at high temperatures.

11.4 Table I Parameter Problems

11.4.1 Reset Level

In order to guarantee the reset of the device over the full temperature range, the reset input voltage must be less than 0.1 VDC. This means that the device cannot be reset reliably by a T^2L output over the military temperature range. In fact, if a T^2L device were used and presented a voltage level close to the reset threshold, device failure could occur, as described in 11.3.5, Device Idiosyncracies.

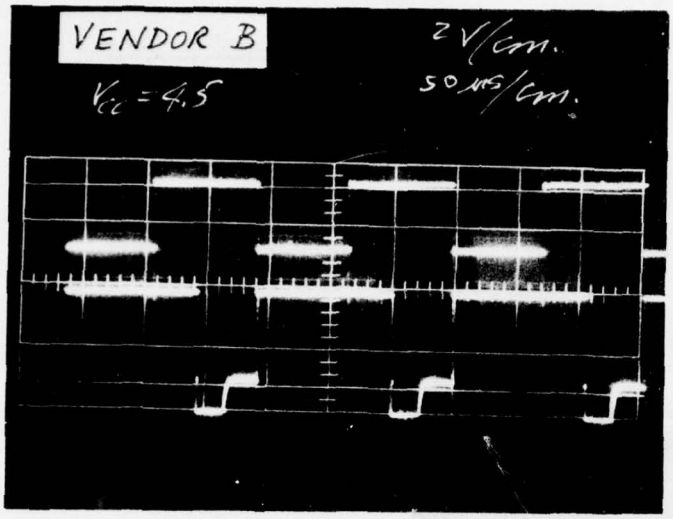
11.4.2 Timing Accuracy

The accuracy in the monostable mode was lowered from ± 1.5% of calculated value to ± 3%. Most vendors did not comment on the originally specified 1.5% even though they all would have experienced a major yield problem.

The accuracy in the astable mode was lowered from ± 2% of calculated value to ± 13% and ± 16% (for charge and discharge times, respectively). The distribution is not centered around the theoretical value for the low speed configuration.

11.4.3 Power Supply Limitations for 556 Dual Timer

The 556 dual timer dissipates more power because it contains two circuits. To avoid excessive dissipation, the designer has set the resistor values slightly higher. This tends to decrease base drive and transistor gain. Thus, the 556 supply level is limited at the lower end to five volts (instead of 4.5 volts) to avoid starving the transistors of base drive and limited at the upper end to 15 volts (instead of 16.5 volts) to avoid excessive power dissipation.

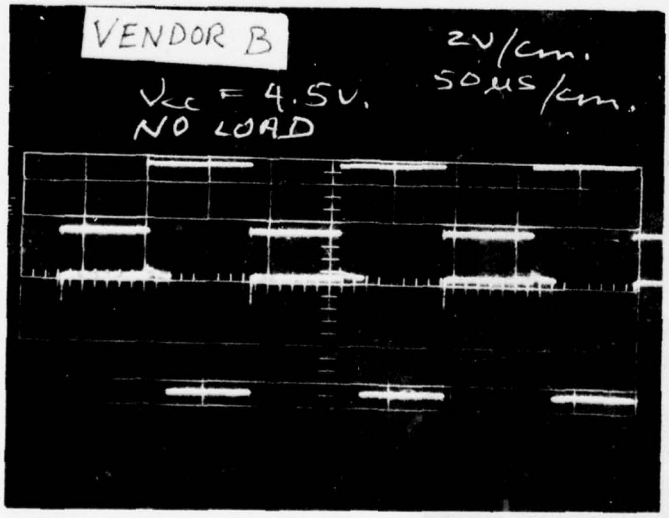


With 300Ω pull-up resistor

Input

Output

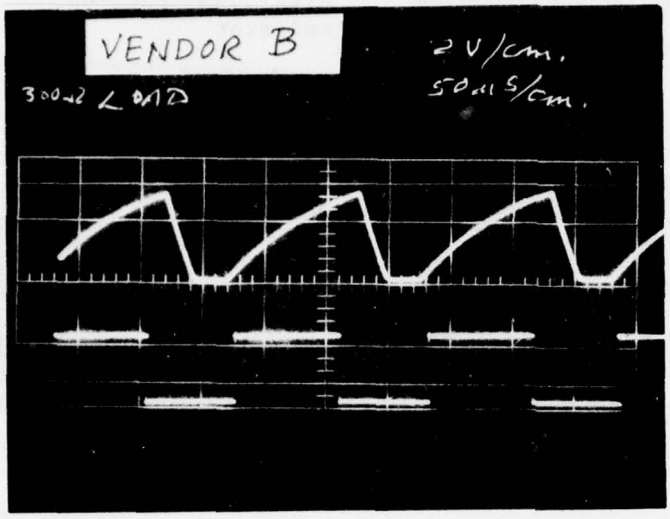
This vendor's device shows dependence on output loading. The output logic "0" step does not occur with no load. The pulse width changes with loading due to an increase in discharge time.



Input

Output No Load

Figure 11-10. Effect of load variation on output logic "0" step.



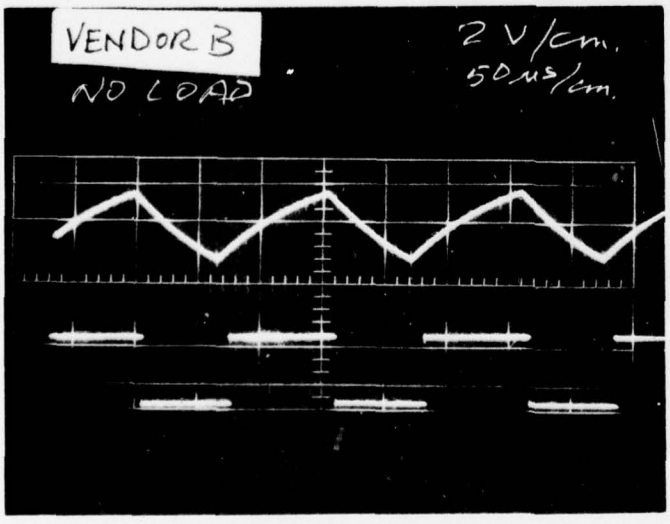
Monostable Mode

R_T = 1 K

C_T = 0.1 uF

Discharge output (V_c)

The 300-ohm load reduces discharge time. The lower photo shows that, without a load, discharge time can exceed 60 microseconds, and premature retrigger results in short charge time.



Discharge outout (V_c)

Input

Figure 11-11. Load dependence of discharge time

11.5 Table I Changes

A comparison of the table I limits (original draft versus final slash sheet) is tabulated in table 11-1. Most of the new limits are based on requests from the manufacturers, especially one manufacturer who actually provided tabulated back-up data for most parameters.

11.5.1 Supply Voltage Changes

The upper end of the supply voltage range for the single timer was lowered from 18V DC to 16.5V DC because the absolute maximum supply level was lowered from 20 to 18. Some margin for variation should be provided to assure device reliability. The 16.5-volt level was chosen because it is 10 percent above the nominal 15-volt supply level. The tighter supply range for the dual timer is discussed in 11.4.3.

11.5.2 Low Level Output Voltage

Besides changing some of the limits on this parameter, a lower level of sinking current was specified to guarantee T^2L compatibility for a specified condition. Also, a 100-microsecond wait before measuring V_{OL} was added to assure no excessive stepping, as described in 11.3.5.1.

11.5.3 Deleted Tests

Two tests were deleted. The Control Voltage Level Test is not necesary because the Threshold Level Test provides some assurance that the control voltage level is correct. The $\Delta V_{TH}/\Delta V_{CL}$ Test is really redundant with Threshold Level Tests at various supply voltage levels.

11.5.4 Addition of a Test

The addition of the Propagation Delay Time, Threshold to Output Test was required to provide a more direct control of an error source for timing accuracy. This delay tends to be an order of magnitude higher than the Propagation Delay, Low to High Level Output (Trigger to Output) Tests. The 12-microsecond limit was chosen based on one manufacturer's request and bench testing at room temperature. One manufacturer had indicated that an eight -microsecond limit would be satisfactory, but bench testing indicated it to be a typical value for that manufacturer's device as well as others.

11.6 Test Circuit Changes

11.6.1 Output Load Changes

The output load changes were made for the dynamic tests. In some cases, the no-load condition is the worst case. The sinking of load current can speed the turn-on time of the discharge transistor by providing extra base drive. Therefore, for the astable timing tests, a no-load condition is the worst-case condition. A load-to-ground configuration could have been used, but one manufacturer requested the no-load configuration due to relay driver

TABLE 11-1. Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	ORIGINAL DRAFT Conditions ELECTRICAL	Other	Limits Min	Limits Max	Units
Power Supply Current	V_{cc} = 4.5 V dc, output low		-	5.0	mA
	V_{cc} = 18 V dc, output low		-	15.0	
Trigger Voltage	V_{cc} = 4.5 V dc	T_A = -55°C	1.30	1.70	V
		T_A = 25°C	1.35	1.65	
		T_A = 125°C	1.30	1.70	
	V_{cc} = 18 V dc	T_A = -55°C	5.70	6.30	V
		T_A = 25°C	5.80	6.20	
		T_A = 125°C	5.70	6.30	
Trigger Current	V_{cc} = 18 V dc	25°C ≤ T_A ≤ 125°	-500	-	nA
		T_A = -55°C	-5000	-	
Threshold Voltage	V_{cc} = 4.5 V dc	T_A = -55°C	2.80	3.20	V
		T_A = 25°C	2.90	3.10	
		T_A = 125°C	2.90	3.10	
	V_{cc} = 18 V dc	T_A = -55°C	11.75	12.25	V
		T_A = 25°C	11.85	12.15	
		T_A = 125°C	11.85	12.15	
Threshold Current	V_{cc} = 18 V dc	25°C ≤ T_A ≤ 125°C	-	250	nA
		T_A = -55°C	-	5000	
Low Level Output Voltage	V_{cc} = 4.5 V dc, I_{sink} = 10 mA	T_A = -55°C	-	.500	V
		25°C ≤ T_A ≤ 125°C	-	.250	
	V_{cc} = 4.5 V dc, I_{sink} = 50 mA	T_A = -55°C	-	2.50	V
		25°C ≤ T_A ≤ 125°C	-	2.20	
	V_{cc} = 13 V dc, I_{sink} = 10 mA	-55°C ≤ T_A ≤ 25°C	-	.150	V
		T_A = 125°C	-	.200	
	V_{cc} = 13 V dc, I_{sink} = 50 mA	-55°C ≤ T_A ≤ 24°C	-	.500	V
		T_A = 125°C	-	.600	
	V_{cc} = 18 V dc, I_{sink} = 100 mA	ALL TEMPS	-	2.0	V

TABLE 11-1. Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	FINAL SPEC CONDITIONS (DEVICE 01/DEVICE 0/2) ELECTRICAL	Other	Limits Min	Limits Max	Units
Power Supply Current	V_{cc} = 4.5 V dc/5 V dc, output low V_{cc} = 16.5V dc/15V dc, output low		- -	5.0/10.0 20/30	mA
Trigger Voltage	V_{cc} = 4.5 Vdc/5Vdc	T_A = -55°C T_A = 25°C T_A = 125°C	1.15/1.30 1.30/1.45 1.30/1.45	1.80/1.95 1.80/1.95 2.10/2.25	V
	V_{cc} = 16.5Vdc/15Vdc	T_A = -55°C T_A = 25°C T_A = 125°C	5.00/4.50 5.20/4.70 5.20/4.70	5.80/5.30 5.80/5.30 6.10/5.60	V
Trigger Current	V_{cc} = 16.5Vdc/15Vdc	ALL TEMPS	-5000	-	nA
Threshold Voltage	V_{cc} = 4.5Vdc/5Vdc	T_A = -55°C T_A = 25°C T_A = 125°C	2.60/2.95 2.70/3.05 2.60/2.95	3.40/3.75 3.30/3.65 3.40/3.75	V
	V_{cc} = 16.5Vdc/15Vdc	T_A = -55°C T_A = 25°C T_A = 125°C	10.6/9.6 10.7/9.7 10.6/9.6	11.4/10.4 11.3/10.3 11.4/10.4	V
Threshold Current	V_{cc} = 16.5Vdc/15Vdc	25°C ≤ T_A ≤ 125°C T_A = -55°C	- -	250 2500	nA
Low Level Output Voltage	V_{cc} = 4.5Vdc/5Vdc I_{sink} = 5 mA	T_A = 25°C T_A = -55°C, 125°C	- -	.250 .350	V
	V_{cc} = 4.5Vdc/5Vdc I_{sink} = 50 mA	T_A = -55°C 25°C ≤ T_A ≤ 125°C	- -	2.60 2.20	V
	V_{cc} = 16.5Vdc/15Vdc I_{sink} = 10 mA	-55°C ≤ T_A ≤ 25°C T_A = 125°C	- -	.150 .250	V
	V_{cc} = 16.5Vdc/15Vdc I_{sink} = 50 mA	-55°C ≤ T_A ≤ 25°C T_A = 125°C	- -	.500 .700	V
	V_{cc} = 16.5Vdc/15Vdc I_{sink} = 100 mA	-55°C ≤ T_A ≤ 25°C T_A = 125°C	- -	2.20 2.80	V

TABLE 11-1 (cont'd). Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	ORIGINAL DRAFT Conditions ELECTRICAL	Other	Limits Min	Max	Units
High Level Output Voltage	V_{cc} = 4.5 V dc I_{source} = -100 mA	T_A = -55°C T_A = 25°C T_A = 125°C	2.4 2.6 2.8	- - -	V
	V_{cc} = 18 V dc I_{source} = -100 mA	T_A = -55°C T_A = 25°C T_A = 125°C	16.0 16.1 16.2	- - -	V
Discharge Transistor Leakage Current	V_{cc} = 18 V dc	-55°C $\leq T_A \leq$ 25°C T_A = 125°C	- -	100 3000	nA
Discharge Transistor Saturation Voltage	V_{cc} = 18 V dc I_D = 100 mA	-55°C $\leq T_A \leq$ 25°C T_A = 125°C	- -	1.2 1.4	V
Control Voltage Level	V_{cc} = 4.5 V dc, V_{OL} & V_{OH}	ALL TEMPS	2.85	3.15	V
	V_{cc} = 18 V dc, V_{OL} & V_{OH}	ALL TEMPS	11.8	12.2	
Reset Voltage	V_{cc} = 18 V dc	ALL TEMPS	0.4	1.0	V
Reset Current	V_{cc} = 18 V dc, V_{OL}, V_R = 0V	ALL TEMPS	-0.75	0	mA
$\frac{\Delta V_{TH}}{\Delta V_{CL}}$	V_{cc} = 18 V dc ΔV_{CL} = 3V (from 12V to 15V)	ALL TEMPS	0.95	1.05	

TABLE 11.1 (cont'd). Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	FINAL SPEC Conditions ELECTRICAL	Conditions Other	Limits Min	Limits Max	Units
High Level Output Voltage	V_{cc} = 4.5Vdc/5Vdc I_{source} = -100 mA	T_A = -55°C 25°C≤ T_A ≤125°C	2.2/2.7 2.6/3.1	- -	V
	V_{cc} = 16.5Vdc/15Vdc I_{source} = -100 mA	T_A = -55°C 25°C≤ T_A ≤125°C	14.0/12.5 14.6/13.1	- -	V
Discharge Transistor Leakage Current	V_{cc} = 16.5Vdc/15Vdc	-55°C≤ T_A ≤25°C T_A = 125°C	- -	100 3000	nA
Discharge Transistor Saturation Voltage	V_{cc} = 16.5Vdc/15Vdc I_D = 100 mA	-55°C≤ T_A ≤25°C T_A = 125°C	- -	1.6 1.8	V
Control Voltage Level	DELETED				V
Reset Voltage	V_{cc} = 16.5Vdc/15Vdc	ALL TEMPS	0.1	1.3	V
Reset Current	V_{cc} = 16.5Vdc/15Vdc	ALL TEMPS	-1.6	0	mA
$\frac{\triangle V_{TH}}{\triangle V_{CL}}$	DELETED				

TABLE 11.1 (cont'd). Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	ORIGINAL DRAFT Conditions ELECTRICAL	Other	Limits Min	Max	Units
Propagation Delay Time, Low To High Level Output	$4.5Vdc \leq V_{cc} \leq 18Vdc$ R_T = 1KΩ, C_T=0.1uf	$-55°C \leq T_A \leq 25°C$ T_A = 125°C	- -	250 350	ns
Transition Time, Low to High Level Output	$4.5Vdc \leq V_{cc} \leq 18Vdc$ R_T = 1KΩ, C_T=0.1uf	$-55°C \leq T_A \leq 25°C$ T_A = 125°C	- -	150 200	ns
Transition Time, High to Low Level Output	$4.5Vdc \leq V_{cc} \leq 18Vdc$ R_T = 1kΩ, C_T=0.1uf	$-55°C \leq T_A \leq 25°C$ T_A = 125°C	- -	150 200	ns
Time Delay Output High (Monostable)	$4.5Vdc \leq V_{cc} \leq 18Vdc$ R_T = 1kΩ, C_T=0.1uf	ALL TEMPS	108.25	111.75	us
	Sames as above except R_T = 1 MΩ	ALL TEMPS	108.25	111.75	ms
Drift in Time Delay vs. Supply Voltage	ΔV_{cc}=13.5V, R_T=1KΩ, C_T = 0.1 uf	T_A = 25°C	-	100	ns/V
Propagation Delay Time, Threshold to Output	NOT TESTED				
TEMP Coefficient of Time Delay (Monostable)	V_{cc} = 18Vdc R_T = 1KΩ, CT=0.1μf	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-8.0 -8.0	0 0	ns/°C
Capacitor Charge Time (Astable)	$4.5Vdc \leq V_{cc} \leq 18Vdc$, R_{TA} = R_{TB}=1K, C_T=0.1	ALL TEMPS	136.0	141.2	us
	Same as above except R_{TA} = R_{TB} = 100KΩ	ALL TEMPS	13.60	14.12	ms
Capacitor Discharge Time (Astable)	$4.5Vdc \leq V_{cc} \leq 18Vdc$, R_{TA}=R_{TB}=1KΩ, C_T=0.1	ALL TEMPS	68.0	70.6	us
	Same as above except R_{TA}=R_{TB}=100KΩ	ALL TEMPS	6.80	7.06	ms

TABLE 11.1 (cont'd). Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	FINAL SPEC Conditions ELECTRICAL	Conditions Other	Limits Min	Limits Max	Units
Propagation Delay Time, Low To High Level Output	$4.5Vdc \leq V_{cc} \leq 16.5Vdc$ for device 01 $5Vdc \leq V_{cc} \leq 15Vdc$ for device 02 $R_T = 1K\Omega$, $C_T = 0.1uf$	$-55°C \leq T_A \leq 25°C$ $T_A = 125°C$	- -	800 900	ns
Transition Time, Low to High Level Output	$4.5Vdc \leq V_{cc} \leq 16.5Vdc$ For Device 01 $5Vdc \leq V_{cc} \leq 15Vdc$ For Device 02, $R_T = 1K\Omega$, $C_T = 0.1$	ALL TEMPS	-	300	ns
Transition Time, High to Low Level Output	$4.5Vdc \leq V_{cc} \leq 16.5Vdc$ For Device 01 $5Vdc \leq V_{cc} \leq 15Vdc$ For Device 02 $R_T = 1K\Omega$, $C_T = 0.1uf$	ALL TEMPS	-	300	ns
Time Delay Output High (Monostable)	Same as above	ALL TEMPS	106.7	113.3	us
	Same as above except $R_T = 100K\Omega$	ALL TEMPS	10.67	11.33	ms
Drift in Time Delay vs. Supply Voltage	$\Delta V_{cc} = 12V/10V$, $R_T = 1K\Omega$, $C_T = 0.1$	$T_A = 25°C$	-	220	ns/V
Propagation Delay Time, Threshold to Output	$4.5Vdc \leq V_{cc} \leq 16.5Vdc$ $5Vdc \leq V_{cc} \leq 15Vdc$ $R_T = 1K\Omega$	ALL TEMPS	-	12.0	us
TEMP Coefficient of Time Delay (Monostable)	$V_{cc} = 16.5Vdc/15Vdc$ $R_T = 1K\Omega$, $C_T = 0.1uf$	$-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 125°C$	-11 -11	0 0	ns/°C
Capacitor Charge Time (Astable)	$4.5Vdc/5Vdc \leq V_{cc} \leq 16.5Vdc/15Vdc$, $R_{TA} = R_{TB} = 1K\Omega$, $C_T = 0.1$ uf	ALL TEMPS	120	156	us
	Same as above except $R_{TA} = R_{TB} = 100K\Omega$	ALL TEMPS	11.3	15.0	ms
Capacitor Discharge Time (Astable)	$4.5Vdc/5Vdc \leq V_{cc} \leq 16.5Vdc/15Vdc$, $R_{TA} = R_{TB} = 1K\Omega$, $C_T = 0.1$	ALL TEMPS	57.5	80	us
	Same as above except $R_{TA} = R_{TB} = 100K\Omega$	ALL TEMPS	5.4	7.7	ms

TABLE 11.1 (cont'd). Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	ORIGINAL DRAFT Conditions ELECTRICAL	Other	Limits Min	Max	Units
Charge Time vs. Supply Voltage	$\triangle V_{cc}$ = 13.5V dc $R_{TA}=R_{TB}=1K\Omega$, $C_T=0.1$	T_A = 25°C	-	250	ns/V
Temp Coefficient of Capacitor Charge Time (Astable)	V_{cc} = 18V dc $R_{TA}=R_{TB}=1K\Omega$, $C_T=0.1$	-55°C ≤ T_A ≤ 25°C 25°C ≤ T_A ≤ 125°C	-25.0 -25.0	- -	ns/°C
Reset Time	V_{cc} = 18Vdc	-55°C ≤ T_A ≤ 25°C T_A = 125°C	- -	250 350	ns
Matching Time Delay Output High (Mono)	4.5Vdc ≤ V_{cc} ≤ 18Vdc R_T = 1KΩ, C_T=0.1μf	T_A = 25°C	-0.1	+0.1	us
Matching Temp Coefficient of Time Delay	V_{cc} = 18Vdc R_T = 1KΩ, C_T=0.1μf	-55°C ≤ T_A ≤ 25°C 25°C ≤ T_A ≤ 125°C	-2.0 -2.0	+2.0 +2.0	ns/°C
Matching Drift in Time Delay vs. Supply Voltage	$\triangle V_{cc}$ = 13.5V R_T = 1KΩ C_T = 0.1 uf	T_A = 25°C	-5.0	+5.0	ns/V

TABLE 11.1 (cont'd). Comparison of Table I Electrical Performance Characteristics for MIL-M-38510/109

Characteristics	FINAL SPEC Conditions ELECTRICAL	Other	Limits Min	Max	Units
Charge Time vs. Supply Voltage	$\triangle V_{cc}$ = 12V/10V $R_{TA}=R_{TB}=1K\Omega$, $C_T=0.1$	T_A = 25°C	-	820	ns/V
Temp Coefficient of Capacitor Charge Time (Astable)	V_{cc} = 16.5Vdc/15Vdc $R_{TA}=R_{TB}=1K\Omega$, $C_T=0.1$	-55°C ≤ T_A ≤ 25°C 25°C ≤ T_A ≤ 125°C	-68 -68	0 0	ns/°C
Reset Time	V_{cc} = 16.5Vdc/15Vdc	-55°C ≤ T_A ≤ 25°C T_A = 125°C	- -	1500 2000	ns
Matching Time Delay Output High (Mono)	5Vdc ≤ V_{cc} ≤ 15Vdc R_T = 1KΩ, C_T=0.1uf	T_A = 25°C	-1.1	+1.1	us
Matching Temp Coefficient of Time Delay	V_{cc} = 15 Vdc R_T = 1KΩ, C_T=0.1uf	-55°C ≤ T_A ≤ 25°C 25°C ≤ T_A ≤ 125°C	-20 -20	+20 +20	ns/°C
Matching Drift in Time Delay vs. Supply Voltage	$\triangle V_{cc}$ = 10V R_T = 1KΩ C_T = 0.1uf	T_A = 25°C	-110	+110	ns/V

limitations of his automatic tester.

11.6.2 Monostable Mode - Charging Resistors (R_T)

The original draft used a one-megohm charging resistor. For the maximum leakage current of three microamperes at 125°C and for the low supply voltage as the capacitor voltage approaches the threshold level, the voltage across the charging resistor approaches 1.5 volts, so that the charging current approaches 1.5 microamperes. Therefore, the device would not operate if its leakage was near the maximum allowed. Even much smaller leakages would degrade accuracy significantly. The one-megohm resistor was changed to 100 K ohms to avoid this problem.

11.6.3 Adapter Test Circuit

The static, monostable and astable test circuits were all combined into one Adapter Test Circuit to reflect the automatic tester configuration more closely.

11.7 Burn-in Test Circuits

No changes to the burn-in circuits were made because there were no comments on those in the original draft.

11.8 Other Specification Changes

11.8.1 Addition of a mini-DIP package

An eight-lead dual-in-line package was added to the Case Outline and Power and thermal characteristics sections as well as figures 1 and 2.

11.8.2 Table II Changes

The following dynamic tests were excluded from 100 percent tests to avoid any requirement for manual tests:

Propagation Delay, High to Low Output
Propagation Delay, Threshold to Output
Transition Time, High to Low Output
Transition Time, Low to High Output
Reset Time

For the group C and D end point, electrical parameters subgroup 1 tests were added to the class B devices.

11.8.3 Table IV Changes

Most of the changes in this table reflect table I changes. The only significant change was the delta limit on I_{CEX} which was increased from ±10 nanoamperes to ± 50 nanoamperes due to repeatability of the automatic tester when measuring a 100-nanoampere current level.

11.8.4 Schematic Diagram of Timer

Circuit A was not changed from that specified in the original draft. However, the "old" version of this circuit which may still be made by some manufacturers, which has the collector of Q10 tied to collector of Q11 instead of ground, exhibits a "no start" failure in the astable mode. The problem is apparently due to the trigger level being very close to zero volts which prevents the base of Q15 from going more than a few tenths of a volt above ground. Thus, Q15 cannot turn on. In any case, the circuit A schematic cannot exhibit this problem.

The circuit B schematic of the original draft was completely deleted from this specification because it does not conform to the operation of all other manufacturers. The manufacturer of this device was advised of this change in the specification and indicated no apprehension. (That manufacturer is of the opinion that the 555/556 timer should not be used in high-reliability systems over the military temperature range.)

The new circuit B schematic is just like circuit A except Q26 and Q27 are used to sink current to ground in the trigger comparator. Q26 operates from saturation with the trigger high to class A with the trigger low. This configuration seems to improve the speed of the device. Bench tests of these devices indicate a generally superior performance to the circuit A configuration.

11.8.5 Addition of Truth Table

The device truth table was added to specify device operation for both manufacturers and users as to what response is expected for all possible input conditions. The device response to one combination of inputs with V_{cc} less than 10V DC varies depending on the manufacturer, but since this is not a normal input state, a simple identification of this variation was considered sufficient.

11.9 Discussion

11.9.1 Potential Problem Areas

The 555 and 556 timers were originally designed to satisfy a commercial marketing need for a low cost versatile one-shot or astable multivibrator. The device application should be very carefully evaluated before being used over the full military temperature range. Some of the main potential problem areas uncovered are summarized as follows:

(1) Lack of T^2L compatibility of the RESET input over full temperature range.

(2) Possible catastrophic failure of the device when a marginal reset level is presented at the RESET input.

(3) Possible double triggering of clock inputs due to output waveform inconsistencies under heavy load conditions.

(4) Dependence of pull-up resistor loading on timing accuracy due to discharge transistor getting base drive from sinking load current.

(5) Excessive leakage current can cause the significant timing accuracy degradation or inoperability with low charging current levels.

11.10 Recommendations for Future Effort

11.10.1 Addition of Special Application Notes

It is strongly suggested that a special application notes section be added to the specification to alert the user to the potential problem areas cited in 11.9.1

11.10.2 Addition of Another Time to the Specification

Because of all the potential problem areas associated with this device, it is further suggested that another timer be added to the specification to provide the user with an alternate device of hopefully higher quality.

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